A Novel Fully Differential Folded Cascode Operational Transconductance Amplifier

S.Kumaravel[1], B.Venkataramani[2], Ajit Randhir[3], Ramakrishna Chowtri[4]

Abstract

In this paper, a push pull differential pair is proposed for enhancement of both gain and unity gain bandwidth of the folded cascode operational transconductance amplifier. The proposed OTA and the fully differential cascoded OTAs reported in the literature are implemented in UMC 0.18μm CMOS Process and studied through simulation. From this, it is found that the proposed OTA has about 25dB higher gain and 100% higher unity gain bandwidth compared to the other OTAs for same load and power consumption. This is achieved at the cost of reduction in the input common mode range by one threshold voltage VTH. The proposed OTA can be used for designing high speed ADCs.

Keywords: *folded cascode, multipath scheme, unity gain bandwidth, inverting current mirror.*

1. Introduction

Operational Amplifiers are the basic building blocks of any analog integrated circuits such as continuous–time filters, variable gain amplifiers, analog to digital converters etc. Designing a high gain and high speed OTA poses a challenge in deep submicron technologies as the reduction in the feature size results in the reduction of the transistor gain factor $g_m r_o$. Since analog circuit performance is strongly dependent on gain and speed, techniques to improve gain and speed are indispensable in deep submicron technologies.

One of the schemes for gain improvement is utilization of cascode configurations. In general, two types of cascode configurations are there namely Telescopic Cascode and Folded Cascode. In telescopic cascade, high gain and high bandwidth can be achieved with less power consumption, at the cost of degradation in the signal swing. But in folded cascode configuration, high gain, high bandwidth and high swing can be achieved at the cost of increase in power consumption. [Sudhir.M.Mallya, Joseph.H.Nevin (1989)] In order to achieve high gain with same power consumption as that of the conventional folded cascode architecture, a multipath scheme which enhances the gain by two fold without much change in the unity gain bandwidth is proposed in [Katsufumi Nakumura, L.Richard Carley(1992)].

In this paper, the architecture proposed in [Katsufumi Nakumura, L.Richard Carley(1992)] is modified at the input differential pair for further enhancement in the gain and the unity gain bandwidth. Section 2 discusses about the conventional architecture. Section 3 briefs about the enhanced architecture in

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INDUCTIVE DEGENERATED LOW-NOISE AMPLIFIER FOR WIRELESS APPLICATION IN 0.18um UMC CMOS

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Abstract

This paper presents the design and implementation of an inductive degenerated common source low-noise amplifier (IDCS-LNA) for wireless applications. All the simulation has been carried out by using UMC RF 0.18um design kit of CADENCE software. The IDCS-LNA has been designed for 2.4GHz and IEEE 802.15.4 ISM band (2.4-2.485GHz) RF frequency range and it draws 7.58mA from 1.8v supply voltage. The same IEEE 802.15.4 protocol band is used in the available ZigBee system. The results obtained from the simulation shows that input impedance of IDCS-LNA close to 50 Ω as well as the optimum values of noise figure and gain obtained for small devices(MOSFET width) (105um) and small drain currents (6.34mA). The designed LNA operated at 2.4GHz shows the gain (S21) of 16.17dB, noise figure (NF) of 2.62dB, output return loss (S22) of -24.98dB, input return loss (S11) of -29.21dB & input 1dB compression point of -15.85dB.In the similar way IDCS-LNA for IEEE 802.15.4 ISM band (2.4-2.485GHz) RF frequency range reflects the gain S21of 15.5 dB, NF of 2.67dB, S11 of -20dB & S22 -16 dB respectively. Also the post layout simulation of same design has been done for 2.4GHz and it exhibits gain of 14.25dB, NF of 3.24dB, S22 of -12.86dB, S11 of -19.97dB.

Keywords: CMOS, low noise amplifier (LNA), impedance matching, inductive degenerated, Sensitivity analysis.

1. Introduction

LNA is considered as one of the most important component or key block in the design of RF receivers. The main function of an LNA is to provide sufficient gain to reduce the noise of subsequent stages (e.g. mixers) while adding as little noise as possible. These two tasks are not always easily achieved simultaneously, the main reason being the noise impedance matching and the input impedance matching are not always obtained for the same source impedance. Therefore, the choice of the LNA topology is very important to achieve the expected performance. Cascode is preferred over other architectures such as common source (CS) with shunt-input resistor, common-gate (CG), and shunt-series amplifiers [1]. In this configuration, the cascode transistor M2 in the common-gate configuration, reduces the parasitic effects of C_{gd} of M1 by presenting a low impedance node at the drain of M1 and increases the stability and linearity.

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A LOW GLITCH CURRENT SWITCH WITH REDUCED SWING AND ITS APPLICATION TO PLL CHARGE PUMP

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Abstract— *A low-glitch current switch is proposed and its application in a conventional CMOS PLL charge-pump is demonstrated. A bias generator circuit enables the current switch to be applied with controlled, limited-swing switching voltages to reduce current glitches due to capacitively coupled spurious charges. The minimum supply voltage to meet head-room and leakage suppression requirements in low voltage deep sub-micron CMOS processes is analyzed. Simulation results on a PLL using this charge-pump show optimized reference spur and rms period jitter down to less than -92 dBc and 0.23 ps respectively for a PLL bandwidth of 2.5 MHz using a 0.35um, 3.3V CMOS process. Measured spur levels on the PLL show reasonable agreement with simulation results.*

Keywords**:** *charge-injection, feed-through, sub-threshold leakage in MOSFET, PLL, charge-pump, glitch, reference spur, pattern jitter.*

I. INTRODUCTION

Current switches that steer a current source into two alternative paths are very widely used in switched-current filters, A/D and D/A converters [1] and in PLL charge-pumps (CP) [2-4]. An important issue in these circuits is current glitches due to capacitive coupling of spurious charges into the sensitive current output node that affects its overall voltage or timing accuracy. For example in the "DOWN" (or NMOS current switch) section of a PLL charge-pump shown in Fig. 1 charge injection or feed-through via C_{gd} and C_{gs} of the switching transistors results in spurious charge to be injected into the loop-filter (LF) resulting in a periodic disturbance or "ripple" [2]at its output. This LF ripple FM modulates the VCO output clock to cause its period to vary over the reference clock cycle resulting in "pattern jitter" or "reference spur"[5].

One method of glitch reduction in current switches that is partially effective [1, 3, 4] is to use dummy transistors to cancel spurious charge coupled through C_{gd} of the switching transistors. Another effective strategy used in [1-4] is to simply reduce the swing of the input voltages of the current switching transistors. Swing reduction not only reduces the magnitude of the spurious charges coupled through C_{gs} and C_{gd} but also results in sharper transition due to smaller slewing current requirement from the driving circuit. Fig. 1 shows a simple scheme for the NMOS current switch. Reduced levels at HI (VH) and LO (VL) are generated by biasing two "diode-connected" transistors at different

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OPTIMIZED FLASH ANALOG TO DIGITAL CONVERTER USING LCT COMPARATOR

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Abstract

This paper proposes 1.8V, 4-bit optimized Flash Analog to Digital converter (ADC) design using Leakage Current Threshold (LCT) Comparators and 2:1 multiplexers with 500 nm technology. In this approach the reference voltages are generated by systematically sizing the transistors of comparator, thus completely eliminating the resistive ladder network required for the purpose. The ADC implemented uses only $2^n/2$ comparators. The circuit of 2:1 multiplexers is implemented to convert thermometer code to binary code. It is observed that with the use LCT Comparator Power Supply Rejection Ratio (PSRR) is improved drastically. The total power dissipation observed is 0.10388 mW.

Keywords: LCT, ADC, Mux.

1. Introduction

Analog to Digital converters with high conversion rate and low power dissipation are becoming extremely important in number of applications. In spite of large number of elements, the flash architecture is one of the best solutions for high speed operation and is also the best for short latency.

The power consumption is one of the most important challenges in transceiver systems and these systems have to be designed to consume as low power as possible due to its power supply limitation. ADC is one of the blocks used in almost any transceiver system. Capacitive interpolation has been employed which gives various advantages when designing for low power circuit [1]. Multiple-selection method where only one section of 4-bit modified Flash ADC is allowed to operate, achieves the aim of low power consumption [2]. A dynamic comparator and interpolation technique has been used in [3, 4] to reduce the power consumption. Through the use of redundancy the low power and high speed ADC is designed in [5]. The conversion algorithm proposed

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Low Voltage Constant Hysteresis Schmitt Triggers

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Abstract

Two new schmitt triggers operating at very low supply voltage which minimize variation in the hysteresis window across process and temperature by using only one type of feedback device are presented: one with only n-type of feedback devices and another with only p-type of feedback devices. The proposed schmitt triggers minimize the spread in hysteresis voltage by eliminating the spread resulting from the variation of process parameters of other type of feedback devices without using any additional compensation circuit or reference/bias voltages and consume no static current. The new schmitt triggers are designed using 140nm CMOS technology and simulation results are presented. The proposed schmitt triggers are targeted at low power designs for control interface applications to detect small variation in the bus voltages by rejecting noise.

1. Introduction

The signals from one device to another device on the board get distorted before entering the receiving device due to noise. Schmitt triggers [1]-[18] are used in I/O interfaces of analog and/or digital systems to increase noise immunity for noisy and/or slow moving signals. Noise immunity is increased by providing hysteresis [10]-[11] which effectively raises the threshold voltage (or switch point) when a logic low is present and lowers the switch point when logic high is present.

The schmitt trigger is a regenerative circuit that incorporates positive feedback. When the input is higher than certain chosen threshold voltage level (V_{IH}), the output is high; when the input is lower than another threshold voltage level (V_{IL}), the output is low. When the input is between these two values, the output retains its state. The difference between the thresholds is chosen such that the input voltage has to change sufficiently to change the output state. This dual threshold action is called hysteresis (V_{HYS}) and defined as the difference between the threshold levels.

In low power [12] systems general approach to save power is to reduce the internal power supply voltage. However, the interface circuits should be capable of receiving high voltage signals from the external world. In such applications, interface circuits built using high voltage devices should be capable of operating

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Design and Analysis of Low Noise Amplifier for WiMAX application

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Abstract

In this paper, a Low Noise Amplifier (LNA) for 2-6 GHz WiMAX application is proposed and designed in 0.13um CMOS technology. Wide band input matching is achieved with a high pass filter at the input in addition to reactive feedback. In the operating frequency range, the maximum NF of 3.6dB, power gain of 13dB, maximum input return loss of –10dB and output return loss of –11dB were achieved. Using the current reuse topology the power consumption of the WiMAX LNA is limited to 5.4mW (excluding output buffer) with a supply voltage of 1.2V.

Keywords (Index): *high pass filter, input matching, WiMAX LNA.*

1. Introduction

High gain, low noise figure (NF) and good input matching are the parameters of interest in a low noise amplifier design. Wide band LNAs used in applications such as WiMAX require the above mentioned parameters to be maintained in the frequency range of interest. Narrow-band inductive degenerated common source LNAs can be converted into a wideband LNA by adding a wideband matching network [M. Ben Amor, M. Loulou, S. Quintanel, D. Pasquet (2008)]. But they take several inductors to achieve wideband input matching and they occupy larger area. The distributed amplifiers [Brian M. Ballweber, Ravi Gupta and David J. Allstot (2000)] used for wide band application but they consume large power and chip area also. So they are unsuitable for low power and low cost applications. The common wideband LNA topologies such as common gate LNA and resistive feedback LNAs can be modified to meet the specifications in the frequency range of interest. Since the NF of a common gate stage is not attractive, the resistive feedback considered here with required modifications. The modifications include the design techniques such as reactive feedback, high pass filtering at input and current reusing.

2. Circuit analysis

The circuit schematic of the proposed WiMAX LNA is shown in Figure.1. A current reuse common source stage gives the required gain. The transconductance of M2 adds to that of M1 to increase the effective g_m of the current reuse input stage with minimum extra current.

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A 110-MHz rail-to-rail amplifier with double-gate MOSFETs

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Abstract

This paper proposes a rail-to-rail amplifier architecture with double-gate MOSFETs, which are possible candidates for CMOS technology nodes beyond 22nm. n- and p-input differential amplifiers are used to achieve rail-to-rail operation. A novel current summing scheme is proposed, for adding the currents of these two differential amplifiers. To accomplish a constant total transconductance for the input stage, the inputs to the n-input differential amplifier are level shifted by -0.2 V, by using a differential amplifier in a unity-gain configuration, whose dc shift is tunable by changing the ratio of widths of the driver transistors. The amplifier achieves a dc gain of 77.5 dB, a unity-gain frequency of 110 MHz at a load capacitance of 10 pF, and a dc power consumption of 285 μW.

Keywords: Rail-to-rail amplifier, double-gate MOSFET, dc level shifter

1. INTRODUCTION

The double-gate MOSFET (DG-MOSFET [1]) is proving to be one of the most promising transistor structures for technology nodes beyond 22nm. DG-MOSFETs have their antecedent in silicon-on-insulator (SOI) MOSFETs, which are now a mature technology (see, for example, [2]). Much research in the technology and physics of DG-MOSFETs has been reported [3–6]. But little has been reported on circuit design. Unique opportunities, and challenges, exist in the design of analog circuits with DG-MOSFETs, due to the flexibility they offer with two independent gates, and their extremely low parasitic capacitances.

Bhatia, *et al*. [7] compared the performance of bulk and DG MOSFETs for designing a low noise amplifier. Jimenez, *et al*. [8], and Alam, *et al.* [9] studied the analog performance of the DG-MOSFET and showed that it will be possible to use these devices effectively until the end of the ITRS roadmap. Having two gates in a single transistor gives the circuit designer an added flexibility, and the possibility of exploiting this flexibility for obtaining better performance. An overview of planar DG-MOSFET physics, technology and circuit performance can be found in [10]. In analog circuit design, the double gate control has been effectively utilized for designing sense amplifiers in SRAMs [11], variable-gain amplifiers and Schmitt triggers [12], and current-mode integrators [13].

In this paper, we report the design of a rail-to-rail constant-G_m amplifier with DG-MOSFETs. A novel scheme is proposed for summing the currents of

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Automating the Design of Successive Approximation Analog to Digital Converters

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Abstract

A systematic automation design methodology is proposed to optimize the power of successive approximation analog to digital converter (SAR ADC). SAR ADC is a mixed signal circuit having both analog and digital sub-blocks. Different varieties of sub-blocks of SAR ADC is thoroughly analyzed and designed using geometric programming as optimization tool. According to the specification, the corresponding sub-blocks are chosen and integrated as the whole ADC. The specifications for the entire ADC is cautiously budgeted among sub-blocks, so that we will get an optimized and accurate design in hand. A computer Aided Design tool is developed to implement the whole optimization process. For a given specification, this tool will give the corresponding design variables for minimum power. This paper, thus giving an abstract level automation tool for SAR ADC which can be improved further. SPICE simulation results of a single ended 12 bits 1 MS/s in a 0.8 um CMOS employing the proposed automation shows that the ADC consumes 0.8 mW and justifies the proposed methodology.

Keywords : Analog to digital converters, SAR ADC, low power, constrained optimization, geometric programming, posynomials.

1 Introduction

Analog to digital converters are the most widely used integrated circuits. Among the ADCs, SAR ADC find place in most applications, because of its moderate characteristics[1]. SAR ADC can be used from very low power applications to relatively high power applications. Designing these two extreme circuits are not the same and needs more time and efforts. Instead if there is any automation method that gives us the design variables while giving just specifications, will make life simpler. This paper is stick to the above mentioned automation and try to give the power optimized, relatively accurate SAR ADC for given specifications. We are using a specific optimization method known as geometric programming.

Many works have been done to optimize both the digital and analog circuits. Automation algorithms used to optimize the circuits can be broadly classified into a) Evolutionary algorithms, a generic population based meta heuristic optimization algorithms like Genetic algorithms and genetic programming [2] ,b) Linear constrained optimization like Integer programming[3], c)stochastic

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Design and Implementation of Differential serial interconnect using Wave pipelining and Surfing

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Abstract

In the literature, surfing and wave pipelining techniques have been proposed for decreasing the delay of interconnects. In this paper, a surfing scheme which uses a "Controllable inverter pair" is proposed for a differential serial interconnect. The performance of proposed scheme is studied through simulation by implementation in UMC 0.18µm technology. Its performance is compared with that obtained for a single ended link using both surfing and wave pipelining. The proposed scheme permits the data transmission rate of 2.5Gbps and it is higher by a factor of 1.875 compared to the single ended scheme. The proposed scheme has the additional advantage of ability to detect stuck-at-faults in either true or complementary links. It also does not require any set up time constraints unlike the single ended scheme which requires about one fourth of the data period.

Keywords*: **Wave pipelining, surfing, differential interconnect serial link, Controllable inverter pair.***

1. INTRODUCTION

As the VLSI technology scales down, transistor sizes get reduced and this in turn increases the speed of the logic blocks [2]. However, interconnects which are used to provide the communication between the logic blocks become the bottleneck. Techniques such as repeater insertion, low swing signaling, wave pipelining has been proposed in the literature to overcome this limitation. However, even with these techniques, the time required to transmit data across a chip may be several clock periods or handshake cycles.

Surfing technique is proposed in ([7],[8]) for improving the reliability of wave pipelined combinational logic circuits. In this technique, a timing pulse called "FAST" propagates along the logic blocks of the wave pipelined circuit. This pulse controls the propagation delay of each block. In particular, the speed of the logic circuits in the data path of the pipeline is augmented by the fast input: asserting fast signal decreases the delay of the logic circuit relative to that when fast signal is not asserted. This paper presents the surfing scheme for wave pipelined differential serial interconnect link.

The organization of the paper is as follows: Section 2 presents the design details of the differential serial interconnect with wave pipelining and the surfing

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Implementation of Embedded Resizing for MPEG-2 Decoder on Trimedia

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ABSTRACT

State of the art In-Car entertainment systems require decoding of MPEG-2 HD broadcast content at lower cost. Decoding MPEG-2 HD content in real time requires high end processing, which would be expensive. However, the car displays are typically of WVGA (800x480) resolution. This provides an opportunity to decode MPEG-2 HD content at lower cost, since we know the rendering resolution is smaller than the content. Embedded Resizing is one such technique, which perform scaling as part of the decoding itself to save number of computations. The computation savings come due to the fact that less number of pixels needs to be processed. However, it introduces a drift in the decoder resulting in gradual degradation of output picture quality. In this paper we introduce an embedded resizing scheme, which provides a good quality output with low drift and at the same time reducing computational requirement. The major highlights of the scheme are using H.264 quarter pixel motion compensation in the MPEG-2 decoder at lower resolution and using spatially aligned filtering matrices for DCT domain scaling for field pictures. These two techniques provide considerably higher picture quality. This decoder was implemented on TriMedia TM3282 media processor. The accelerated instructions for H.264 motion compensation on TM3282 helps in keeping the computational complexity lower. Data cache misses are also reduced due to inherent lower resolution in the decoder. As a result of all this, we get a HD MPEG-2 decoder, which provides good quality lower resolution output suitable for the display and at 30% lower computation requirement. This paper describes the embedded resizing scheme used and results achieved.

Index Terms *– MPEG-2,* decoding, *media processors, low cost, software implementation, TriMedia.*

1. Introduction

Typically the car display is of WVGA (800x480) resolution and the input can be a HD resolution (1920x1080 or 1440x1080). Since the full resolution of HD cannot be exploited on lower display resolution, there is a need to scale the video to lower resolution. Traditionally the content is decoded and then scaled to lower resolution. To save computational load, efficient scalable video decoding algorithms can be used, which will decode the video in the reduced resolution with good video quality. The algorithm embeds the scaling directly at

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3.3-V Signaling with 2.5-V Devices Using Dynamic Biasing

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Abstract

A new 3.3V signaling circuit topology using 2.5V device in 65nm CMOS process technology is presented. This paper describes the principle of dynamic biasing technique to avoid transistor gate-oxide breakdown and hot carrier degradation without using any additional reference or bias voltages. This principle is targeted at low power design by avoiding any static currents. The concept is explained with respect to inverter circuit. This principle can be easily applied to any other digital circuit operating at higher voltages than the devices support.

1. Introduction

For conventional CMOS circuits in the static condition, the gate-source, gate-drain or drain-source voltages for both NMOS and PMOS are equal to supply voltage. The conventional CMOS inverter consists of a PMOS (M1) and NMOS (M2) is shown in Fig.1. In this kind of circuit, the steady state output (V_{OUT}) and input (V_{IN}) voltages will take one of the logic states high or low. In both cases, the gate-source, gate-drain or drain-source voltages of both transistors are equal to VDD or 0V depending on the logic state of the inverter [1].

In advanced CMOS processes all the transistor dimensions get smaller in order to increase the performance (speed) while reducing the cost (area). Simultaneously, the maximum tolerable voltage across transistor terminals decreases to ensure life-time [2]-[4]. In 65nm standard CMOS technology, IO devices can tolerate up to 2.75V (2.5V nominal) across gate-source, gate-drain or drain-source without any reliability issues like oxide breakdown [2] or hot carrier degradation [3] [4]. To comply with standardized protocols, many circuits in advanced CMOS process must work at higher voltage than their nominal supply voltage. For example, 3.3V signaling is required to comply with USB standard [5] and circuits need to be designed with 2.5V devices. If the conventional CMOS inverter is operating at 3.3V and is fabricated using 2.5V devices then both transistors will experience the stress, which will cause lifetime reliability issues like hot carrier degradation or gate-oxide breakdown.

The general topological approach used to design high voltage circuits using low voltage devices is to cascode the devices as shown in Fig.2 [6]. The cascode device gates are connected to intermediate voltage (ngate and pgate) to avoid the high voltage stress on the devices. These intermediate voltages are selected such

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A Design of Experiment based Approach to Variance Optimal Design of Analog Circuits

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Abstract

The effects of random variations in the fabrication process have increased significantly with the scaling of technology, causing analog circuit performance parameters to deviate from their expected values. This leads to parametric failure of IC performances causing a significant loss of yield. In this work a new design approach has been presented to minimize the effect of process variations and random mismatches between transistor pairs on circuit performance. A statistical design flow, with the goal of enhancing the parametric yield for robust design, has been adopted based on response surface methodology (RSM) and design of experiment (DOE) techniques. Stochastic MOSFET (SMOS) models have been used for statistical simulation of circuits to capture the effect of process variation and mismatch in terms of performance parameter variation. Using the developed quadratic response surfaces for variance of performance parameters, device sizes have been optimized to get a variance optimal design keeping other performance parameters as design constraints. The efficiency of the proposed flow has been validated using designs of a two-stage operational amplifier and an LC voltage controlled oscillator.

Keywords: *Process Variation, Mismatch, Variance Optimal Design, Design of Experiments, Response Surface Methodology, Voltage Controlled Oscillator*

1 Introduction

Manufacturing process variation and random mismatch between devices with the scaling of technology lead to uncertainty in the analog circuit performances causing a significant amount of yield loss. Due to increasing difficulty in controlling the variation in different fabrication steps such as gate-oxide growth, channel and source-drain implants, photo-lithography and etching etc in sub-micron technology, designers need to consider these effects on performance deviation. In order to produce manufacturable analog integrated circuits with high functional yield and a high degree of reliability, the design of the circuit should be robust with respect to process and device parameter variation [1].

To address the increasing difficulty in manual design, during past two decades, many statistical design optimization approaches have been proposed to

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Simulation of 22nm n-Metal Oxide Semiconductor Field Effect Transistor

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Abstract

Process Simulation of 22nm n-Metal Oxide Semiconductor (n-MOS) Transistor is done using Synopsys TCAD (Technology Computer Aided Design). For this simulation, Halo Implantation and Silicidation processes are used. Halo Implantation is done to reduce Drain Induced Barrier Lowering (DIBL) effect and Threshold Voltage (V_t) roll-off. Silicidation is carried out to decrease the source/drain shallow junction resistance. High-k dielectric is used for reducing the leakage current density. The 22nm n-MOSFET simulated in the present work shows a drive current of 398.35uA/um at gate voltage of 0.8V with a subthreshold slope of 88mV/decade and the threshold voltage of 0.23V.

Keywords (Index): *22nm nMOS Transistor, Process and Device Simulation, Synopsys TCAD, Scaling*

1. Introduction

As the dimensions of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are scaled down, the switching speed is improved and the power dissipation is reduced [1]. Both the factors are of great importance as the present day's requirement is high speed switching for faster circuits and improved operation speed; at the same time, low power dissipation is important to preserve battery life of electronic gadgets [2]. Scaling of devices also results into the increased packing density to facilitate more and more devices in a given chip area and increased functionality in the same area of a single chip [2-5]. This reduces the price per chip and hence price of electronic gadgets. In fact, over the past 30 years the number of transistors per chip has been doubled every 2-3 years once a new technology node is introduced [6].

As the gate length of MOSFETs is scaled down to 22nm, the impact of short-channel effect, High-field effect, quantum effect, parasitic resistance/capacitance, the process variation and heat dissipation becomes noticeable [7]. It is essential to maintain a constant electric field for reliability of these devices, which is attained through voltage scaling [1]. The constant voltage scaling also lowers the transistor power, needed to maintain constant power density.

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VLSI Architecture and FPGA Implementation of Image Enhancement Algorithms for Medical Images

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Abstract

Image enhancement is an important task in the field of image processing and is widely used in real time medical imaging systems that are used for diagnosis. A number of these systems do not produce good visual quality image that hinders the diagnosis of disease. Major attributes of these systems include real time speed and robustness. These systems also require Post-processing of the acquired images in order to improve the visibility or detect ability of the image features. The required post-processing can be done using a high speed general purpose processor (GPP) that comply with the speed requirement of these systems, but they are sensitive to the hard onsite environment conditions and also consume a significant amount of power. Dedicated hardware processing unit allows these systems to do the processing on the fly (on capture) and are robust as compared to the GPPs. In this paper, we propose a pipelined VLSI architecture of the image enhancement algorithms applicable to medical images. The implementation of these architectures onto the Xilinx SpartanIII FPGA is also included in this work. Enhancement results of these algorithms, on application to medical images for diagnosis are presented here. We also present the analysis and comparison of the hardware and operating speed of the proposed architectures in this work. The proposed architectures can easily be embedded on the existing medical imaging systems and hence enhance the speed and robustness of the complete process significantly.

Keywords — Image enhancement, FPGA.

Introduction

Image enhancement is a process that improves the quality (clarity) of the image for a particular task. Removing blur and noise, increasing contrast, and revealing details are examples of enhancement operations. Image enhancement approach fall into two broad categories: Spatial domain and frequency domain [1]. The term spatial domain refers to the image plane itself and approaches in this category are based on direct manipulation of pixels in an image. Frequency domain processing techniques are based on modifying the Fourier transform of an image. The spatial domain algorithms have less complex hardware and hence are computationally faster in comparison to the frequency domain algorithms. Thus, in this work we address implementing the first category of algorithms that will improve the computational speed of the imaging system significantly.

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DEVELOPMENT OF A BIRD'S EYE VIEW PARKING ASSISTANCE SYSTEM ON A PROGRAMMABLE MULTIMEDIA PROCESSOR

Bijo Thomas[1], Yann Picard[2], Rajiv Chithambaran[3], Cecile Cougnard[4]

Abstract

Development of a parking assistance system on a programmable multimedia processor and its implementation challenges are described. A prototype of the parking assistance system based on the proposed architecture was constructed. The details of the system including, hardware architecture, software architecture are described. Finally, the visual and performance results generated using the prototype developed are provided.

Keywords: Fish Eye models, projection, bird's eye view, optimization

1. Introduction

Parking assistance systems that present to the driver a bird's eye view (overhead view) of the car and its surroundings is an effective aid when parking and in slow driving scenarios. In such systems, images of the vehicle's surroundings are captured using multiple fish eye (wide angle) cameras mounted on the car, and the captured images are processed using image transformation techniques. The transformed images are joined together to form the bird's eye view image of the car and the surroundings and this image is displayed. A bird view is a synthetic view of the immediate surrounding of a car, as though it were captured by a bird positioned right above the vehicle. The main purpose of this view is to provide the driver with parking assistance.

Methods for processing multiple camera images of the vehicle surroundings for display to the driver are known in literature, for example from the papers [1][2], as well as from various patent applications such as [3], [4]. Parking assistance using a multi-camera infrastructure is disclosed in [5]. Most of the computing architecture solutions available in the literature are based on FPGA or ASICs or weakly programmable solutions [6], [7], [8]. A high performance, programmable solution for bird view processing is relevant since this reduces the cost of the automotive electronics system to which the bird view belongs. The bird view system described here is a highly optimized solution implemented

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A Method to Reduce Switch-On Delay in Miller Based Slew Rate Controlled IO

Dharmaray Mallappa Nedalgi and Kiran Gopal

Abstract

Miller capacitor is used for slew control in IO cells. For significant slew rate control, it is required to connect large capacitor or make the pre driver too weak. This slows down transition time and also has an unsolicited effect of increasing the propagation delay of the IO cell. The initial time taken to charge the capacitor till the threshold voltage of the output transistor is significant part of this propagation delay. This paper presents a way to avoid the initial time required to charge the huge Miller capacitor and thus achieve higher slew control without increasing the propagation delay of an IO cell.

Keywords (Index): *Miller compensation, Slew rate control, Switch on delay*.

1. Introduction

For low to medium speed IO pads in typical VLSI designs, slew control is a must [1]. At higher drive strengths, the fast changing IO voltage may create current spikes resulting in EMI interference. The high current drain creates noise in power supply limiting the maximum simultaneously switching cells that per supply pair. An easy way to add slew control is a Miller capacitor. The added advantage of a Miller capacitor is that slew control is load independent [2] - [4].

2. Miller Control Operation

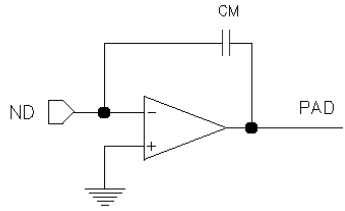

Fig. 1. Op-Amp Integrator with current input.

Architectural Power Management for Battery Lifetime Optimization in Portable Systems

Manish Kulkarni[1] **and Vishwani D. Agrawal**[2]

Abstract

For portable computing devices, maximizing battery lifetime or performing maximum possible operations per recharge is a primary objective. Various voltage and frequency scaling techniques are being used in commercial devices. This work considers the role of energy source, i.e., battery, in the optimization of a portable system. We introduce battery lifetime in number of clock cycles as an optimization metric. In addition the energy consumed by the system, battery lifetime also depends upon the battery efficiency, which may degrade as the power consumption increases. We examine power reduction techniques for a processor such as frequency scaling, i.e., clock slowdown (CSD) and instruction slowdown (ISD) from a battery efficiency viewpoint and estimate battery lifetime expressed in number of operational cycles. In case of ISD, implemented with the help of NOPs, we demonstrate that the lifetime for a given size of battery might be optimum at a slowdown factor around 2 to 3. The battery lifetime improvement requires reduced power dissipation coupled with prolonged execution time and, surprisingly, sometimes even increased energy consumption. With architecture level modifications, such as instruction slowdown, battery lifetime increase of 20% is realized.

Keywords: Battery lifetime, Portable electronics, Power management, Clock slowdown, Instruction slowdown

1. Introduction

Computing platforms have become exceedingly more portable over time. Moreover, contemporary mobile computing devices are capable of performing as many computations per second as that of desktop computers few years back. Fortunately, due to technology scaling and power efficient approach in design, these mobile devices do not consume as much power as that of desktop computers. But with increasing usage of mobile devices in everyday life and the variety of applications being performed by these devices, the demand for power from power sources is continuously growing. Using a battery of higher capacity is not a solution, since for portable devices, the size and weight of battery, which are proportional to the battery

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Tied-Gate DG-FinFET based Radiation Tolerant SRAM Cells

S. S. Rathod[1], A. K. Saxena[2], and S. Dasgupta[3]

Abstract

Protection of SRAM against ionizing radiations is utmost important when it is used in mission critical applications. Nowadays SRAM cells are designed with advanced devices like Double-Gate (DG) FinFET. However, memory protection has not yet been realized enough for designs manufactured in advanced technologies. In this paper, several types of circuit level techniques are proposed to enhance the immunity of SRAM cell to ionizing radiations. Five different types of 32 nm DG-FinFET based SRAM cells are analyzed and the best structure has been proposed. Static Noise Margin (SNM), Read Noise Margin (RNM), Write Noise Margin (WNM) and Power Delay Product (PDP) are the performance metrics computed for each type of SRAM cell. Benchmarking has been done against 'Dual Interlock Cell' (DICE) structure.

Keywords: Single Event Upset, SRAM, Simulation, Radiation Effects

1. Introduction and Background

The errors caused by cosmic rays and alpha particles remain the dominant factors causing errors in electronic systems. Radiation induced errors in microelectronic circuits are caused when charged particles lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs [Wang at al. (2008)]. SRAM is used in several electronic designs for storing critical data. SRAM when used in space or nuclear applications is required to have both high operating performance and good hardness to radiations. SEU in SRAM is the dominant contributor to the overall soft error rate (SER). Nowadays, several designs techniques are used mainly to protect on-chip SRAMs and register files. At the circuit level, increasing the critical charge of a circuit node and adding transistors to enable redundant storage of information are two main approaches to reduce the effects of soft errors [Hirose at al. (2002), Hite at al. (1992), Ioannou at al. (2003), Actel (1997), Calin (1996), Liu at al. (1992)]. These techniques tend to increase the power consumption and lower the speed of the circuits. These designs usually require at least twice as many transistors as unprotected circuits, which typically

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BER Analysis of Flip-Flop and Latches with Wire Pipelining

Devendra Giri[1], Gagnesh Kumar[2], Diwakar Singh[3]

Abstract

In this paper a detailed analysis for how the number of flip-flops and latches inserted are affecting BER and repeater size with wire pipelining is performed. Here it has also been illustrated that there is a lower bound for the power consumed by a certain interconnect pipelining scheme. Since number of flip-flops, latches and repeater sizes cannot scale down beyond a certain limit due to the solidity requirement, which is determined by maximum allowable bit error rate (BER). This makes a new contribution to reduce BER while increases number of Flip-Flops, Latches and Repeater size.

Keywords: Bit Error rate (BER), Timing Margin (TM), D-flip flop, Wire Pipelining.

1. Introduction

Building a sequential machine requires memory elements which read a value, save it for some time and then write that stored value somewhere else even if the element's input value has subsequently changed. A Boolean logic gate can compute values, but its output value will change shortly after its input changes. Each alternative circuit used as a memory element has its own advantages and disadvantages. A generic memory element has as internal memory and some circuitry to control access to the internal memory. Access to the internal memory is controlled by the *clock* input. The memory element reads its *data* input value when instructed by the *clock* and stores that value in its memory. For interconnect delays beyond the capabilities of repeater insertion, several alternative approaches can be adopted to meet certain timing constraints [1][3][5][6]. But all these approaches have their own drawbacks. Insertion of sequential elements in interconnects lines – a concept that is become known as *interconnect pipelining* – is one feasible solution for modern nanometer technologies. The idea is to divide a wire, whose delay is longer than one clock cycle, into several segments by inserting sequential elements to store signal values that require multiple clock cycles to travel through a particular global wire.

2. BER Analysis for Flip-Flop Based Wire pipelining

The Solidity of wire pipelining scheme is strongly dependent on many factors including repeater sizing, process, parameter variations and clock signal variation. Some of the factors cannot be controlled, such as the clock signal variation and the wire delay uncertainty. The BER can be decreased by changing

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Critical Charge Model for Novel Radiation Tolerant Flip-Flop

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Abstract

With the continuous downscaling of CMOS technologies, reliability due to single event upset (SEU) has become one of the major bottlenecks in the evolution of next generation systems. This paper presents critical charge model for the novel radiation tolerant flip flop. Circuit level technique has been used to reduce the effect of SEU during static data storage phase in the flip flop. The technique used in this paper outperforms in terms of critical charge, 'Mean Time Between Failure' (MTBF) and an area as compared to the other types of methods used to harden the flip flop like 'Triple Module Redundancy' (TMR), 'Built in Soft Error Resilience' (BISER) and 'Sense Amplifier Based' flip flop. The results for the critical charge obtained from the proposed analytical model are contrasted against HSPICE simulation results. A close match was found which validates the proposed model.

Keywords: Single Event Upset, Simulation, Circuit Design, CMOS, Degradation

1. Introduction and Background

Protection against single event upset (SEU) is very important for space, biomedical, and communication applications [Maiz at al. (2005)]. Wide spread use of the pipelined architectures in modern digital systems do requires a large number of flip flops and latches. Hence design of the radiation hardened flip flop becomes necessary to make the digital systems more reliable in the presence of ionizing radiations.

At the circuit level, increasing the critical charge of a circuit node and adding transistors to enable redundant storage of information are two main approaches to reduce the effects of radiations. Techniques namely TMR [Actel (1997)], sense amplifier based [Wang at al. (2004)] and BISER [Zhang at al. (2006)] are reported. Flip flop sizing scheme and flip flop variants that function as low-pass filters for transients [Joshi at al. (2006)] and use of multiple V_{dd} [Lin at al. (2007)] are also reported. Redundant circuit techniques include the low power cell [Liu at al. (1992)], Barry design [Barry (1992)], Dooley Design [Dooley (1994)], and DICE [Calin (1996)]. The DICE (dual interlocked cell) design is one of the best known classical circuit level hardening techniques. These

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HALO IMPLANT PHOTORESIST MASK LAYER SHADOW EFFECT ON LEAKAGE IN 65nm SRAM CELL

H. C. Srinivasaiah[1]

Abstract

Leakage characteristics of 65nm MOS devices were studied in a 0.594μm^2 SRAM cell as a function of halo implant photoresist (PR) mask layer thickness, for embedded memory application. The photoresist mask layer thickness has been varied from 100nm to 600nm in steps; in response to this variation, the leakage and drive (ON state) currents are observed to increase significantly. In pull down NMOS transistor, leakage currents increased from 2.3nA to 93nA, while the drive current increased from 0.14mA to 0.2mA, in saturation region of operation, at device width W_n=120nm. For pull up PMOS transistor, the saturation region leakage currents increased from 0.08nA to a maximum of 0.15nA with the drive currents increasing from 20μA to a maximum of 24μA with device width W_p=90nm. This case study has been conducted at cell/device V_{dd}=1.2V and at a fixed halo tilt angle $\theta = 30^o$ for a customized 65nm SRAM process recipe, targeted for low power.

Keywords: *Photoresist shadow effect, Low standby power, Leakage currents, Halo implantation, Embedded SRAM, 65nm process technology, Low power SRAM, and Process integration.*

I. Introduction

Modern Microprocessor Units (MPUs) have multi-level cache memory to achieve increased throughput [1, 2]. Low power embedded memories are built using low standby power (LSTP) technologies [3]. Accordingly one approach to achieve low standby power is to add sleep transistors providing virtual ground for memory cells, thus reducing the leakage in standby mode [3, 4]. Embedded SRAM cache achieves lower latency but they are the power hungry elements [1]. Integration of on chip SRAM consuming low operating power and low standby power is very challenging due to the issues that are arising from lithography and etching process steps with scaling [5].

The leakage currents in SRAM affects the half selected row and half selected column bits resulting in bit failure during read/write operations [1, 6, 7]. Thus it becomes imperative to study the leakage behavior of a process technology used to manufacture complex ICs [5, 8, 9].

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A (1/5.5 x V_{DD}) to (3/2 x V_{DD}) BIDIRECTIONAL I/O BUFFER AT 0.35µm, 3.3V CMOS TECHNOLOGY USING INNOVATIVE INPUT RECEIVER

Arnab K. Biswas[1] and S. Dasgupta[1]

Abstract

In this paper a new fully bidirectional I/O buffer using 0.35µm CMOS technology is proposed. Many conventional buffers suffer the problem of gate oxide overstress. The proposed buffer solves the problem by controlling the junction voltages within 3.3V which is the normal rating for 0.35µm devices. The proposed buffer can work with a wider range of voltages i.e. 0.6/0.9/1.2/1.5/1.8/2.5/3.3/5 V utilizing less silicon area than which has been reported till now. For the first time, to the best of our knowledge 0.6V bidirectional buffer has been proposed in this paper. In addition, a new innovative input receiver is proposed which uses less number of MOS transistors than which has been reported in literature till now. The whole I/O buffer uses only standard 0.35µm thin oxide devices, so no extra process cost is required as well.

Keywords: *Bidirectional Buffer, Innovative input receiver, 5V to 0.6V range, I/O Buffer with transmitter and receiver*

1. Introduction

The input/output (I/O) circuits are essential to VLSI chip design. There are various problems faced by bidirectional buffers like gate oxide overstress, hot carrier effect etc because of the lower supply of the buffer and the higher pad voltage [Dabral and Maloney (1998)]. To solve these problems, there can be technological solutions as well as innovative circuit design solution. Technological solutions include dual oxide process, use of separate n-well bias etc [Chen and Ker (2007)]. However, the use of thick gate-oxide devices not only increases the cost of wafer fabrication, but it also changes the threshold voltages of the pull-up/pull-down transistors. Separate n-well bias also causes some problems like layout routing problem, body effect etc [Chuang and Ker (2004)]. Therefore, generally innovative circuit design techniques are used. These techniques include the use of different circuit blocks like floating n-well circuit, gate tracking circuits etc. But it increases complexity and it also requires a lot of silicon space. Recently a bidirectional buffer was reported which can work with a wide voltage range from 0.9V to 5V [Wang, Hsu, Liao and Liu

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Self Timed System Design Using FIFO.

Dr. R.K.Sharma[1] ,Dr. A.K.Gupta[2] ,Mansi Jhamb[3], Vinod Kumar Khera[4]

Abstract

Globally Asynchronous Locally Synchronous (GALS) Systems have provoked renewed interest over recent years as they have the potential to combine the benefits of asynchronous and synchronous design paradigms In this paper we propose applying GALS techniques to FPGAs in order to overcome the limitation on timing imposed by slow routing.

Keywords: CLOCKLESS, Asynchronous, FIFO, Clock distribution

I. INTRODUCTION

Increasing number of gates and clock speed is the trend of semiconductor industry these days. Synchronous designs run by a single clock implies difficulties with clock distribution and excessive power consumptions. The field of synchronous-to-asynchronous circuit conversion (a subarea of the asynchronous design style) is in the same situation as the whole asynchronousdesign style. Numerous approaches for automated conversion of synchronous-to asynchronous circuits have been proposed in recent years. However, none of them has matured enough to become an industry standard adopted by EDA tool producers. Each of the existing approaches (according to the extent of the author's knowledge) has its specific advantages and drawbacks, but none of them can really generate asynchronous circuits with all the so often claimed advantages (clock skew avoidance, power efficiency, modularity of design, better than worstcase performance, lower EMI, adaptation to environmental variations, higher security), totally beating the clocked circuits. Especially, when considering parameters like performance, power consumption and circuit's size. Most systems (embedded / FPGAs) are designed with one or moreglobal clocks. FPGAs with multiple clock domains must provide some mechanismfor synchronising data passing between them, which will increase latency and be prone to metastability. One solution is to pipeline the routing, as used in[1]. A potential problem of this is that the number of clock cycles allocated to the routing must be determined at the routing stage and may impact upon any cycle allocation assumed at the circuit design stage. Also, concurrent data travelling along different routing paths need to contain exactly the same number of pipeline stages or data will arrive on different cycles. In this paper we propose adding asynchronous routing to a synchronous FPGA. This paper will detail a new method that is used to design, synthesize and analyze a safe FIFO between different clock domains using Gray code pointers that are synchronized into a different clock domain before testing for "FIFO full" or "FIFO empty" conditions.

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PERFORMANCE ANALYSIS OF CARBON NANOTUBE INTERCONNECTS

Tafseer Alam[1], Rohit Dhiman[2] and Rajeevan Chandel[3]

Abstract

From 45nm technology node problems like scattering, increase in resistivity and electromigration occur in copper (Cu) interconnect. At 45nm technology node dimensions of Cu interconnects come into the range of mean free path of electron (~40nm) that is why these problems come in to the picture. So there is need of an interconnect material which can replace Cu from 45nm technology node. Carbon Nanotube (CNT) can be used as interconnect because of having superior properties like mean free path, current carrying capacity, thermal stability and mechanical strength. Mixed CNT bundle has various parameters viz. average diameter of tube, tube density, inner to outer diameter ratio and probability of metallic tubes inside bundle. This work shows that proper selection of these parameters leads tominimum bundle resistance at 32nm technology node. A comparative analysis of power and delay with variation of driver resistance and load capacitance has also been shown. This analysis has been carried out for CNT bundle and Cu at 500µm and 1000µm. It is found that power and delay of CNT bundle are smaller than corresponding Cu interconnect. This is the advantage for CNT interconnects. It can be said that CNT is better replacement for interconnect in ultra large scale integration (ULSI).

Keywords: Carbon nanotube, copper, delay, interconnect, power.

1. Introduction

Interconnect will play very important role in future technologies. Interconnects provide power supply, ground, clock and essential signals to integrated circuit [1]. The size of transistors is reducing with technology scaling. So to connect these transistors on chips, the interconnect size must also be smaller. It means with downscaling there is also a need to scale down the dimensions of interconnects. But this theory gives good performance only up to 45nm technology node. Below 45nm Cu faces serious problems of increase in resistivity, electromigration and grain boundary & surface scattering. These problems occur because Cu dimensions enter the range of mean free path of electron in Cu. To eliminate these problems thinner Cu wire is necessary in lower technology nodes. Since current conventional process to fabricate Cu wire

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Optimisation of lateral Silicon Nanowire based Solar cell using 3D TCAD Simulation

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Abstract

Nanowire structured solar cells have shown promising potential for integrated power source for nanoelectronics systems such as driving element for nano-wire sensors, logic gates etc. Further recent theoretical studies have indicated that solar cell having junction in radial direction has better solar cell performance characteristics than its planar counterpart. In this study we report the 3D TCAD simulation study of lateral p-type/intrinsic/n-type (p-i-n) coaxial silicon nanowire (NW) solar cell. The performance of NW solar cell is benchmarked with planar structure of same dimension under AM 1.5G solar spectrum. With the help of TCAD doping density of p-core, n-shell and the thickness of intrinsic shell are optimized. The effect of using low quality material on NW solar cell performance is also investigated. Simulation results show that lateral nanowire solar cell give highest open circuit voltage (Voc) and short circuit current (Isc) for n-shell doping density of 10^{19} cm^{-3} . We find that p-core doping density variation does not have significant affect on Isc, while Voc increases and get saturated at about doping density of 10^{18} cm^{-3}. We get the best efficiency for i-shell thickness of 80 nm. Simulation result shows that the defect density of about $10^{14}cm^{-3}$ can be tolerated without losing significant amount of efficiency. These results can be used as guidelines for designing nanowire based self powered integrated circuits.

Keywords: Nanowire Solar cell, Cell efficiency, Build in field

1. Introduction

Semiconductor nanowire shows some excellent properties like large surface to volume ratio which can be utilized in solar cells. Nanowires have already found its use in organic [1], dye-sensitized [2], quantum-dot sensitized [3] solar cells. Different groups [4] [5] have shown that solar cell having junction in radial direction works more efficiently as compare to its planar counterpart. Even with the low quality material it gives sufficiently high output. Similarly Bozhi Tian et al. has physically fabricated lateral p-i-n nanowire based solar cell in self powered circuits and reported the efficiency of around 3.4 percent [6]. Different groups [7] [8] have also fabricated vertical nanowire based solar cell using bottom up approach but the efficiency reported in other studies is quite low.

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CLUSTER BASED ROUTING FOR MULTI PIN DROPLETS IN DIGITAL MICROFLUIDIC BIOCHIPS WITH INTELLIGENT COLLISION AVOIDANCE

Pranab Roy[1],Hafizur Rahaman[2],Parthasarathi Dasgupta[3]

Abstract

Microfluidics based biochips are comprised of microfluidic arrays based on rigid substrates through which, movement of fluids is tightly controlled to facilitate pre scheduled biological reactions.In modern day biomedical applications digital microfluidic biochips find major uses in the areas of medical diagnostics, drug design, DNA sequencing etc. Simultaneous droplet routing poses a hard problem for design automation of digital microfluidic biochips (DMFB). The droplets are planned to be routed concurrently as well as constrained for route timings to avoid cross contamination. This paper attempts to solve this problem for multiple source and target locations with the objectives of minimizing the electrode usage, as well as the latest arrival times. A Hierarchical method guided with problem specific heuristics towards dynamic path selection for intelligent collision avoidance is proposed, and experimental results are found to be encouraging as compared with other techniques.

Keywords: Micro fluidics, Digital Microfluidic biochips, algorithms, routing, clusters.

1. Introduction

With the advancement of Microfabrication technology digital microfluidic Lab on Chip offers an enhanced platform for developing diagnostic applications in the areas of high-throughput DNA sequencing, immunoassays,environmental toxicity monitoring, and point-of care diagnosis of diseases.Microfluidic devices are designed from the bottom up,whereby various fluidic components are combined together to form a device that performs a multitude of applications.The classical concept of microfluidics, i.e., the confinement of the flow of single phase liquids to networks of narrow channels, has some fundamental drawbacks. The most obvious one is the fact that in small dimensions, the Reynolds number Re of the flow rarely exceeds unity, such that the flow is purely laminar (the threshold for turbulence is Re > 200). As a consequence, mixing two substances is difficult, and may proceed only by diffusion or, in some cases, be achieved via viscous dephasing. Hence, there has been considerable development towards the use of isolatedwater droplets suspended in an oily phase. The main advantage considered in this context is the twisty flow pattern emerging within the droplets when they are moved through the channel system. Mixing of two aqueous components is achieved in this way within each droplet separately, and is found to proceed quite efficiently Electrowetting has been used successfully as one of several techniques used to actuate microdroplets in a digital micro fluidic device. In most applications electowetting allows large number of droplets to be independently manipulated under direct electrical control without the use of pumps, valves or even fixed channels. ElectroWetting-On-Dielectric (EWOD), is a method which is based on changing the wettability of liquids on a dielectric solid surface by varying the electric potential. This method offers advantages over conventional continuious flow microfluidic chips, by way of significantly reduced sample size, as well as reconfigureabilty and scalability of architecture. In analogy to digital microelectronics, these basic instructions can be combined and reused within hierarchical design structures so that

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Low Power High Throughput Differential Current Mode Signaling Technique for Global VLSI Interconnect

Sujeet kumar[1], R.B. Deshmukh[2], R.M. Patrikar[3]

Abstract

Global interconnect face significant challenge to dense Very Deep Submicron (VDSM) Systems–on-Chips (SoC), due to increasing wire delay. Hence interconnection technique which decreases delay and power, play an important role in future technologies. The proposed differential current mode signaling circuit decreases delay and power by providing overdrive current during signal change. The results obtained from the simulations shows a low voltage swing of 150mV at receiver, average power dissipation of 121 u W, delay 220 p sec. and throughput 4.74 GHz for 5mm interconnect length.

Keywords (index): *Current mode signaling, Differential signaling*

1. Introduction

As technology scaled down number of transistors integrated onto a single die has increased. The technology scaling trends indicate that, the delay of local interconnects is tracking the delay of transistors but the delay of global interconnects is increasing. This is becoming a major bottleneck in the realization of systems on-chip. Using low-resistivity materials like copper and low-K dielectric provides some improvements but as the technology scales to [1]smaller dimensions the delay through a fixed length wire continues to increase.

The conventional approach to deal with the interconnect delay problem is buffer insertion. By adding buffers or repeaters to the long wire, the delay becomes linear with respect to length. [1-2] used the concept of optimum number of repeater insertion for the performance improvement of on-chip RLC interconnects. [3-5] discussed the voltage scaled repeater insertion methodology for global interconnect for high throughput and low power interconnect. All these methods introduces area problem. However, there is a limit to the performance improvement that can be obtained with repeaters in deep submicron designs in terms of power and delay. With the advancement in technology, chip size is reducing and on-chip interconnection complexity is

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On-Chip Test Circuits for Throughput Measurement of High Speed Interconnects

Amit J. Vishnani[1], **Marshnil V. Dave**[1], **Maryam S. Baghini**[2], **and Dinesh K. Sharma**[2]

Abstract

In this paper, two new on-chip test circuits to characterize the throughput of high performance on-chip interconnects are presented. One of them uses a random bit sequence and the other uses a pre-selected worst case data pattern. The circuits are designed and laid out in 180nm CMOS technology. With the proposed schemes, Bit Error Rate (BER) of the order of 10^{-12} can be measured for interconnect schemes operating at data rates as high as 1.7 Gbps even in the worst process corner and at 2Gbps for a nominal process corner. As the basic component of the test circuit is a flip-flop, a new pulse based flip-flop has been designed to achieve high operating speed. Simulation results of the RC-extracted netlist shows that maximum operating frequency is 3.33 GHz in the nominal process corner. Accordingly the proposed flip-flop operates at 10% higher frequency while dissipating 12.1% less power, compared to other state of the art high speed flip-flops.

Keywords: *State-of-the-art Flip-Flop, On-Chip Test Circuits, High Speed Interconnect Circuits, Throughput, Bit Error Rate.*

1. Introduction

Performance of on-chip interconnects has been a major bottleneck to the performance of VLSI circuits. To overcome this bottleneck, recently very high speed on-chip interconnect schemes have been proposed [1-3]. Off-chip measurement of throughput (maximum rate at which data can be transmitted) of the interconnect schemes requires large on-chip buffer which consumes high power. Further, sophisticated instruments are required to view the eye opening or to measure BER. Hence on-chip measurement circuits are preferred.Most on-chip measurement circuits follow one of the following three approaches for performance characterization.

(a) Delay measurement method [3]
In this approach, latency of the interconnect scheme is measured and inverse of the delay is considered as throughput. This measure of throughput is inad-

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Layered Test bench Framework for Verification

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Abstract

This paper presents a novel approach of test bench framework enabling complete reusability leading to reduced verification time and effort. A layered framework has been proposed to simplify the test-bench design and enable re-use on layer by layer basis. In total it constitutes five horizontal layers and two vertical layers. These layers range from lowest level of utilities till highest level of test vectors. This framework fetches advantages of test-bench reuse, re-using test vectors across different platforms for example RTL, SystemC etc, monitoring facility, logging and debugging facility, usability as a traffic generator, ease in extendibility, support to multiple abstractions and finally contributing to significant reduced verification time and effort.

Keywords: Verification, test bench framework, re-usability

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CATD: A tool for Consistency Analysis of Timing Diagrams

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Abstract

In recent times, assertion based verification has assumed a significant role in the design validation industry for verifying implementations of protocol models. An assertion based verification routine typically takes as input an implementation model for a given protocol and a set of correctness requirements and verifies whether the implementation satisfies the requirements. Timing diagrams have been used as a representation of protocol transactions for a long time. In this paper, we propose a methodology for automatically verifying whether a given protocol timing diagram complies with an assertion suite for the same protocol. We have developed a prototype tool for consistency checking of timing diagrams with respect to an assertion suite. Experimental results on industry standard protocol specifications show that our approach works well in practice.

INTRODUCTION

In industrial practice, timing diagram is a common form of specifying signal values and transaction level behavior for protocol standards. Due to its simplicity of representation and visual appeal, timing diagrams have grown in popularity and are found in almost every specification document. A timing diagram for a protocol specifies the precedence and timing dependencies among a set of signals participating in a transaction over a finite period of time. Over the years, a number of variants of timing diagrams have been developed.

In the last decade, Assertion based verification (ABV) has become a wide-spread methodology in the design verification community for verifying correctness of protocol models. An assertion based verification routine typically takes as input an implementation model for a given protocol and an assertion suite and verifies whether the implementation satisfies the assertions.

In this paper, we propose to solve a different verification problem, that of checking whether a timing diagram specification of a protocol is consistent with the set of assertions for the same protocol. Our proposed method for consistency checking builds on the foundations of assertion rewriting and incremental unfolding with value substitutions popularly used in Bounded Model Checking (BMC) [6] procedures. Intuitively we extract the signal valuations and dependencies from the timing diagram model and evaluate the assertions to check whether the assertions evaluate to true or false.

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Simulation of Low Voltage Flash Memory Cell

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Abstract

Simulation of Conventional floating gate flash memory cell and Quantum dot floating gate flash memory cell for 90nm technology is carried out using Synopsys Technology Computer-Aided Design (TCAD) software. The advantages of quantum dot flash memory cell are explored through the simulations. Critical issues such as, programming, erasing of flash memory, its substrate current and charge storage characteristics are studied through TCAD simulation. Hot-carrier injection model is used for charge injection into the quantum dot electrode and Fowler-Nordheim tunneling model to study the erasing behavior. Substrate current is calculated using shockley read hall (SRH) Field Enhancement model and Avalanche generation model. All these simulations are carried out at low voltages in optimum time. The quantum dot based flash memory cell is expected to be more reliable than the conventional floating gate flash memory cell. The simulations also suggest that the former are faster and can be operated at lower voltages than the latter.

Keywords (Index): *flash memory, floating gate, quantum dot, control gate, low voltage, faster, reliability*

1. Introduction

Today the market demands faster, smaller and more reliable electronic and optical devices. Some novel structures such as nanocrystals, nanorods and nanotubes are being explored to achieve these benefits in the conventional devices [1]. Among these, quantum dots are quite popular due to the exceptional characteristics. In quantum dots charge confinement occurs in 3-dimension, this confinement effect brings new and unique properties that can be utilized in devices to import better performance and new functionalities.

One of the promising applications of quantum dots is in flash memory devices where the conventional floating gate is replaced by an array of quantum dots. Flash memory is a non volatile memory that can be programmed and erased electrically. Today's flash memory cell consists of polysilicon floating gate, which is the data-storing element of the memory cell. In flash memory cell data is stored in the form of electrical charge which gets accumulated in floating gate depending on the voltage applied on control gate. Higher control gate voltage results in larger amount of charge on the floating gate. To change the

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FOOLPROOF METHODOLOGY TO VERIFY CLOCK-STOP IN SOC

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Abstract

Scan based debug is widely used post-silicon debug methodology. It is an important feature for post-assembly-line debug as well. Pre-silicon verification of this feature takes center stage due to the above reasons. Recently, considerable verification bugs relating to the feature were missed in pre-silicon verification and found in silicon. Many of these bugs were related to stopping of functional clocks. After due diligent investigation of such bugs, it was discovered that the dimension of verification involved here was considerable since clock gating could be spread all over the chip and every design choose to implement a different flavor of clock gating. Moreover, it is a challenge to identify 0-delay glitches and errant clock edges that could compromise the state of the design. In this paper we showcase sample bugs, contrast different verification methodologies and suggest a foolproof methodology to verify clock-stop.

Keywords: Scan, Scan based debug, Scandump, Functional clock stop

1. Introduction

Scan based silicon debug is a well known methodology to debug silicon pre/post production. It is a reliable methodology to debug most functional failures. Hence pre-silicon verification of this feature is high on priority. One major source of bugs related to the feature occurs during stopping of functional clocks in the design. Such bugs could manifest themselves as stray/ free-running-clocks, clock gating miss at target cycle and glitches in clocks. These bugs could fatally disturb design state and hinder post-silicon debug. Verification challenge is to make sure that design is stopped cleanly and without any glitches. The dimension of this problem increases when multiple IP components are used at SOC, which choose to use different flavors to clock gating. A particular IP could even choose to implement non-deterministic clock gating with deterministic maximum slip-cycles. Such IPs provide checkers to instrument SOC verification, and to assert the functional correctness of clock gating at SOC.

In this paper, we present verification misses by prior verification efforts and present improved verification methodology which is foolproof to catch bugs related to functional clock gating and scan based debug.

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Performance Optimization of FinFET for Ultralow Power Circuits

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Abstract

Subthreshold circuits are attracted by the battery operated handy devices for achieving the longer battery life time. Subthreshold operation of Si-MOSFET causes increased delay and variability problems. DG FinFETs are promising device even in subthreshold region which overcomes most of the limitation of Si-MOSFET. Subthreshold circuit shows very low power dissipation but at the cost of speed, however further improving the speed can increase the application area of subthreshold circuits. 3T DG FinFET provides higher performance with lowest subthreshold slope and better Ion/Ioff ratio. This paper investigates the effect of change in width, channel doping concentration and tsi on FinFET device and circuit performances. Further optimized 3TADG is compared with conventional 3TSDG and it is observed that optimized 3TADG perform well in terms of delay with loss of some switching energy.

Keywords: DG FinFET; Subthreshold logic; Ultralow power; Channel doping concentration.

1. Introduction

Continuous scaling down of CMOS has enabled high performance and low power VLSI circuit design possible. However, Medical equipments such as hearing aids and pace-makers and wireless sensors, cellular phones required extremely lower power consumption [1], [2]. For these applications high speed is not required. Research interest in subthreshold circuit design has been greatly increased in recent few years due to pressing demand for ultralow power consumption by the handy equipments. To reduce the power consumption one of the most commonly used technique is to scale the supply voltage, scaling of supply voltage is continued even below to the threshold voltage of device to achieve the ultralow power dissipation by using the subthreshold leakage current as switching current. Along with ultralow power, subthreshold circuits are greatly benefited by small gate capacitance, high transconductance and hence better noise margin and voltage transfer characteristics. Since magnitude of subthreshold leakage current is very low in the range of few nano amperes which limits the operating frequency range of subthreshold circuits. Improving the performance of subthreshold circuits will extend the application area and will able to contend the superthreshold circuits with low power design. This paper mainly contributes towards improving the speed of subthreshold circuits.

Digital circuits designed using double gate devices has been shown more power efficient than the same circuits implemented in bulk CMOS at same gate

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On-Line Detection of Crosstalk Fault in FPGA Using BIST Model

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Abstract

In this work, we have developed a BIST model to detect crosstalk fault in FPGA. The crosstalk causes signal delay, logic hazard and circuit malfunctioning caused by interference between interconnects although they are electrically isolated. All possible causes of the crosstalk due to capacitive coupling, inductive coupling or both between a pair of lines have been considered. The work presents a new BIST model that requires lesser overhead as compared with earlier techniques. It is found that the proposed detector can detect any logic hazard or delay due to crosstalk. Hence this model can be utilized for effective diagnosis of crosstalk faults using minimal overhead. The proposed scheme is simulated in MATLAB and verified using Xilinx ISE tools and Modelsim 6.0.

Key words: *BIST, crosstalk, FPGA, delay, interconnects, fault detector, diagnosis.*

1. INTRODUCTION

With advancement of VLSI technology, the feature size shrinks and device becomes smaller and faster. However the wire resistance and capacitance decreases at much slower rate, even in some cases increases proportionately resulting in wire delay. Hence interconnect wires which are electrically isolated, are in fact some times interfered with each other and the effects have an impact on system performances. The effect caused by interference between electrically isolated interconnects is known as crosstalk. This crosstalk can cause additional signal delay, logic hazard and circuit malfunctioning. Hence the effects of crosstalk must be considered during design validation. As the spacing between interconnect wire decreases, the coupling capacitance becomes the dominant source for overall wire capacitance. With the increase of clock speed and decrease in rise time, the inductance becomes an important factor for signal integrity and signal delay. With increase in wire length (long wire), the effective current loop is increased making mutual inductance effective. As the coupling capacitance and inductance affect the performance of the device in deep submicron technologies, the crosstalk becomes a serious problem that needs to be addressed both from the manufacturers and designers point of view.

Recent works [2] are focusing towards investigation of the crosstalk noise in FPGA. Various methods have been proposed to minimize the effects of delay [3-7]. An analytical model of the crosstalk due to coupling capacitors has been presented [3] in which the detailed mathematical analysis of crosstalk due to capacitive coupling has been explained. A method to detect glitches and delays in transition due to crosstalk noise in FPGA is proposed in [4]. Here, a BIST technique to detect crosstalk faults without extra overhead has been used. In [5-6], a self-checking method has been used for online testing of transient and crosstalk affecting the interconnection of synchronous system implemented in FPGA. The system has self-checking property that makes it suitable for high reliability requirements. The technique in [7] discussed a test-per-

Design of RF Low Noise Amplifier using CMOS technology at 2.45 GHz

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Abstract

This is a design of RF low noise amplifier at frequency of 2.45 GHz using CMOS technology. The main aim of the design was to achieve low noise figure at improved gain with the help of CMOS technology. This has become possible by using single stage nMOS transistor and it is the novelty of this design. The noise figure of the circuit is 1.201dB with forward voltage gain coming out to be 22.915dB. Design is working at 11.2mA drain current with supply voltage of 3.3 V & biasing voltage of 1.48V

Keywords: *Low Noise Amplifier(LNA), Noise figure(NF), Scattering parameters (S parameter)*

INTRODUCTION

RF low noise amplifier is the front end block of the receiver system. Signal coming from the antenna is directly given to the low noise amplifier. External as well as internal noise of the circuit is reduced, so that the signal with maximum strength can be received .

Achieving good result for design of RF IC's with CMOS technology has become an area of interest. CMOS technology has given shape to digital IC development. If RF/Analog ICs can also be designed efficiently with CMOS technology, it will solve the issue of making separate IC's for analog applications. It will allow to manufacture both analog & digital blocks of the communication system with same technology.

Thus this design has used CMOS technology. NMOS transistor has been used with its BSIM model. This design has been made specifically for Bluetooth application. Characteristics & specifications of LNA for Bluetooth applications have been listed in below table:

Characteristic	**Specification**
Gain	>12 dB
Noise figure	< 3dB
Center frequency	2.45 GHz

Table1:Characteristics & specifications of LNA for Bluetooth applications

As per above mentioned requirements, this design satisfies all characteristics with its specifications. Gain & noise figure have been tasted by making S-parametric simulations .

General design equations for design of low noise amplifier can be considered as follows

Input impedance is given as,

$Rin=Rg + Ls\ gm/Cgs +j(wLs – 1/wCgs)$

It can be rewritten as,

$Rin = Rg + Ra + j[Xls –Xcgs]$

Where $Ra= Ls\ gm/Cgs$

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Investigation of Linearity Performance of a Double Gate Band to Band Tunnel Field Effect Transistor

Rakhi Narang[1], Manoj Saxena[2], R. S. Gupta[3] and Mridula Gupta[1]

Abstract

Linearity and analog performance of MOSFET is well studied. However there has been no discussion about linearity and analog performance of tunnel field effect transistor (TFET) which could help in finding a niche and suitability for tunnel FETs in the analog and RF application arena. Since in RF applications devices with better linearity and a low distortion are required, so it becomes necessary to assess the various linearity and distortion Figures of Merit (FOM) such as VIP_2, VIP_3, IIP_3 and IMD_3 and analog performance metrics such as g_m/g_d and g_m/I_{ds}. In the present work, a silicon based DG-TFET is analyzed for its linearity and analog performance and a comparison is made with a DG-MOSFET using ATLAS 3D device simulation software. Further a low bandgap material SiGe is also considered in order to overcome the issue of low drive current in TFETs and its effect on the Linearity and analog parameters is also investigated.

Keywords: DG-TFET, FOM, Linearity, SiGe

1. Introduction

Continuous scaling of CMOS in order to achieve high speed of operation, very low power dissipation has been the driving force for the booming electronic industry. The ever increasing demand of consumer electronics, wireless communication and computing has led to mixed mode circuits integrating digital and analog circuitry on a single chip forming System on Chip (SoC) circuits. Although with shrinking dimensions the cut off frequencies of the order of 100 GHz and more can be attained and thus making CMOS technology suitable for RF applications but the increased Short channel effects (SCEs) degrades the output resistance (R_{out}) and hence deteriorating the intrinsic gain performance [1-2]. In order to overcome these issues, new device structures and material systems must be studied. One of the novel device structure based on a rather

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Analog Performance of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET: Simulation study

Vandana Kumari[1], Manoj Saxena[2], R.S. Gupta[3], and Mridula Gupta[1]

Abstract

In the present work RF linearity of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET is analyzed using ATLAS 3D device simulation software and is compared with the insulated shallow extension (ISE) MOSEFET and Silicon On Nothing (SON) MOSFET. Comprising ISE architecture on to the existing SON MOSFET leads to the suppression of short channel effects (SCEs) along with the amendment of device efficiency (g_m/I_{ds}), voltage gain (g_m/g_d), output resistance (R_{out}) and other linearity coefficients like VIP_2, VIP_3 and IIP_3. It is demonstrated that with the ISE structure incorporated onto the existing SON MOSFET and tuning of various parameters such as shallow extension depth (X_e), pillar thickness (T_{si}) shows excellent short channel immunity and better linearity performance.

Keywords: Linearity, MOSFET, Insulated Shallow Extension, Simulation.

1. Introduction

Better operating speed and lower power consumption ability make the MOSFET dominant in the field of Analog and Digital Circuit design due to aggressive scaling [1].The performance of the CMOS transistors have improved dramatically due to their miniaturization made possible through the advancements in device technologies [2]. Compared to traditional CMOS bulk technologies, Silicon On Insulator (SOI) technology are utmost acceptable as alternative technology that could lead to a better trade-off between active and leakage power [3]. The main difference between the bulk and SOI substrate is that the buried oxide layer located below the active silicon layer [4]. Therefore each transistor can be electrically isolated from each other [5]. Properties of the device can further be enhanced by replacement of oxide layer with air (i.e. Silicon On Nothing) [6], which results in the reduction of parasitic to the greater extent due to the lower dielectric constant of air than the SiO_2.

Various advanced lateral channel engineering techniques such as super halo [7], steep source/drain junction [8] are proposed to further reduce the short channel effects (SCEs). However, tremendous increase in band to band drain leakage current limits the usage of these profiles. Thus, dielectric pockets, which have a

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A Wide Temperature Range (50- 500K) Analysis For the Nanoscale Surrounding Cylindrical Gate MOSFET with Localised Charges

Rajni Gautam[1] , Manoj Saxena[2], R.S.Gupta[3] and Mridula Gupta[1]

Abstract

Abstract--In this paper a wide temperature range analysis for the nanoscale cylindrical surrounding gate MOSFET with localised charges is presented. The effects of variation in temperature (50–500 K) on the electrical characteristics of the both damaged and undamaged nanoscale SRG MOSFET due to hot carrier induced localised charges at the Si-SiO_2 interface have been studied. The study includes the effects of temperature on the threshold voltage, subthreshold current, drain current and subthreshold slope of the device.

Keywords: ATLAS-3D, hot carrier effect, interface traps, localised Charges, SRG MOSFET

1. Introduction

In order to realize high packing density and high cut-off frequency for future ULSI design, both the channel length and channel width must be reduced. A decrease in channel length leads to SCEs, whereas reduction in channel width causes a reduction in current drive capability These problems lead to scaling limitations on conventional single and double gate MOSFETs. Surrounding-Gate (SRG) MOSFETs have been recognized as one of the possible choices to boost CMOS performance beyond the conventional scaling limit. SRG MOSFET has large effective channel width even in small-occupied area as the sidewalls of the pillar are used as transistor channel region. Also, the gate length is adjusted by the height of the silicon pillar without changing the area of the transistor thus offering high shrinkage features Thus it offers short-channel-effect immunity, suppressed floating body effects, improved transport property, and CMOS compatibility. The modeling of SRG MOSFETs requires a different approach compared with conventional bulk CMOS due to unique physical effects of the SRG MOSFETs such as volume inversion. Recently, extensive study of SRG

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STUDY OF ENERGY EFFICIENCY OF SINGLE PHASE ENERGY RECOVERY LOGIC WITH PROGRESSIVE TECHNOLOGY

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Abstract

This paper presents the extensive study of energy efficiency of single phase energy recovery logic circuits with progressive technology. The energy recovery logic is a best candidate for achieving the goal of energy efficient CMOS design. It is necessary to study the energy efficiency of such logics with technology scaling. The single phase energy recovery logic family members like Clocked Adiabatic Logic (CAL) and Source Coupled Adiabatic Logic- Diode connected (SCAL-D) are studied. The circuits are simulated at TSMC 180nm, 90nm and 45 nm CMOS technology nodes and energy efficiency is analyzed with signal frequency and supply voltage variations. The results have been compared with logically equivalent static CMOS circuits. This research work proves the functionality of energy recovery logics at modern technology node.

Keywords: low power, energy efficient CMOS design, energy recovery logic

1. Introduction

The low energy electronics circuits are most demanding in this era. As packaging density is continuously increasing, the heat sinking problem became of concern. Various solutions have been suggested for ultra low power at device, circuit and system levels [1]. The energy recovery logic design is best candidate for achieving ultra low power that significantly reduces the energy consumption and ultimately the heat generation. These circuits recover the undissipated energy related to charges stored in device parasitic capacitance and resistance and recycle though an efficient resonant power supply.

Over the past two decades, various energy recovery logic circuit families have been proposed [2]-[7], these circuits are categorized as: multiphase energy recovery logic and single phase energy recovery logic. Both circuits are able to achieve significant energy saving over static CMOS counterparts. But, in multiphase energy recovery circuit design, multiphase power supply clock distribution is used that increases the overall circuit complexity and clock network energy loss. Thus, multiphase energy recovery circuit design is

ANALYSIS OF SERIES RESISTANCE IN SI-NANOWIRE FET

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Abstract

The cylindrical gate-all-around (GAA) silicon nanowire field-effect transistor is a promising device structure for the 22-nm CMOS technology node. However due to small wire diameter, these devices suffer from a high series resistance. The series resistance of GAA devices is extracted using geometry-based analytical model, which is validated using three dimensional device simulations. The series resistance extraction is done by dividing it, into spread resistance, sheet resistance and contact resistance. The extraction technique is applied in nanowire device at 22 nm channel length with different source/drain extension lengths of 15, 20, 25, 30, and 35 nm, respectively. The proposed analysis well characterizes the essential parameters influencing the series resistance and the relative contribution of the device/process parameters on the total series resistance. It is found that the spreading resistance due to the lateral doping gradient contributes significantly to the series resistance.

Keywords: series resistance, Gate-All-Around, nanowire

1. Introduction

Gate-All-Around (GAA) Si-nanowire FET is one of the most promising candidates for the downscaling of CMOS, since the surrounding gate allows an excellent electrostatic gate control of channel charges, and hence reducing short-channel effects [1]–[3]. As channel length scales, the channel resistance becomes correspondingly small. However, the extrinsic series resistance does not scale proportionately and is becomes a significant part of the total device resistance. Since the series resistance has become the critical issue owing to its source/drain extension doping gradient and contacts [3], [8]. The series resistance extraction in GAA FET devices have been reported [2], [5], [6]. L. choi *et al.* [6] reported the extraction of series resistance using mobility degradation model for long channel length devices. The series resistance extraction using Y-function technique has been reported by Rock-H baek *et al.* [5]. In Y-function technique a good linearity of transconduntance versus gate voltage is required at low V_{DS}. However, a parabolic shape of transconductance with change of gate voltage has also been reported by [7] and hence, the Y-function technique could not predict the series resistance for all cases. An alternative technique for analyzing the series resistance is to use the three-dimensional geometry-based analytical model [4], [8]. The series resistance is

LOW POWER SWITCHING ACTIVITY ON SCAN BASED TESTING VECTOR USING FOLDING METHOD

S. Saravanan[1] and Har Narayan Upadhyay[2]

Abstract

Present complexity of VLSI design is increasing rapidly in the number of test patterns and the corresponding data transition time. This large test data volume is becoming one of the major problems in association with huge switching activity and its corresponding response time. This paper considers the problem of huge switching activity in scan based test pattern. This proposed folding algorithm is based on reducing the huge switching activity on scan shift in operation. This is achieved by equally folding the scan based test pattern, which is used for testing. Each scan test pattern is folded into equal necessary blocks. This reduces the overall switching activity of the flip-flop in the design. Theoretical analysis and experimental results on ISCAS89 shows that the proposed method reduces the total switching activity of the test pattern by 75% when compared to the traditional approaches.

Keywords: Test pattern, Folded Blocks, Switching activity

1. Introduction

Today's System on Chip (SoC) complexity continues to grow in size, increasing data volume and cost of the manufactured chip testing in the semiconductor industry. This huge integrated complexity challenges the scan based testing of sequential circuits with flip-flops used in scan based design becoming one of the major power consuming devices. Shift operation for loading and observing the test data leads to excessive transition in the corresponding flip-flop. This excessive transition in primary input increases the power consumption and reduces correlation between consecutive test pattern including the unnecessary switching activities of circuit signals.

Power dissipation achieved in the test mode operation is much higher than normal mode of design operation [1]. In normal mode operation very small design portion of the flip-flops will change the value during each and every clock pulse. But in test mode operation huge number of flip-flops will change the value. Due to this huge change in flip-flops it produces more switching activity. This increases the problem of huge heat dissipation and more transition time.

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Behavioural Analysis of Clock Jitter Effects in Continuous Time Sigma Delta Modulator

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Abstract

This work presents a system level modelling of clock jitter influence on second order continuous time sigma delta modulators with Cascade of Integrators Feed Forward (CIFF) architecture. It incorporates a technique for faster jitter simulation and helps to predict various design parameters like oversampling ratio (OSR)and out of band gain (OBG) for the required resolution and SNR with Non Return to Zero (NRZ) and Switched capacitor Resistor (SCR) feedback DAC shapes. It analyses the SNR degradation of the modulator in the presence of jitter. Simulation results show a reduction of jitter sensitivity by 4dB with SCR feedback technique. Optimum OBG and OSR are found to be 1.5 and 128 respectively for a resolution of 12-bits.

Keywords: *Clock Jitter, switched capacitor resistor, out of band gain*

1. Introduction

The emergence of powerful digital signal processors implemented in CMOS VLSI technology creates the need for high resolution analog-to-digital converters. Sigma deltas (ΣΔ) ADCs provide higher resolution with low power dissipation and moderate sampling rate. But as the speed increases, various non-idealities come into picture, out of which, clock jitter is a prime concern as it reduces the signal-to-noise ratio of the modulator. It is shown in [O.Oliaei and H. Aboushady (1998)] that the variation of pulse width is worst effect of jitter.

Various techniques have been reported in literature [Maurits Ortmanns, Yiannos Manoli (2002)] for jitter sensitivity minimization. The basic idea behind all these techniques is to provide a sloping pulse instead of a rectangular one so as to reduce the amplitude of feedback signal during sampling instant. This in turn reduces the amount of jitter introduced. The sloping pulse may be generated from the output using a capacitor and a resistor. Hence the technique is called as Switched Capacitor Resistor [Maurits Ortmanns, Yiannos Manoli (2002)] feedback technique.

Circuit level implementation of SCR feedback for Continuous Time (CT) ΣΔ ADC is considered in [Maurits Ortmanns, Yiannos Manoli (2002)]. A quantitative analysis of the effect of both NRZ and SCR feedback on the jitter sensitivity in ΣΔ modulators are studied and compared in this paper. In order to speed up the simulation, the technique proposed in [A. Ashry and

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Wireless System Design and System Engineering Challenges

Muralidhar Bandi; **Kameswara Rao B**; **Ajith Kumar V K**;
and **B. Ravi Kishore** (HCL Technologies, Chennai, India)

Cordinating Presenter: Dr. B. Ravi Kishore

Topics Covered:

(1) Introduction to Wireless Communication
(2) Basic Concepts in Radio Frequency (RF) Engineering
(3) Modulation Techniques – A Brief Overview
(4) Wireless System Design
(5) Wireless Transceiver architectures
(6) Design Case Studies
(7) Trends and challenges in wireless system design
(8) Conclusion

Tutorial Summary:
Pervasiveness of wireless technology is impacting every aspect of the society and is becoming a de facto feature of any electronic product. This tutorial provides a comprehensive overview of wireless system design and brings out the system engineering issues through real-life design case studies. It begins with an overview of a typical wireless system and the underlying RF technology. Next, a detailed view of wireless system design with mathematical underpinning of concepts and design of sub-systems will be presented; it highlights systems engineering issues in wireless product development. Subsequently, the tutorial presents the relevant system design case studies, for various wireless applications viz; medical electronics, consumer electronics telecommunications etc., and explains the methodologies to address the systems engineering issues. The tutorial explains the trends in future wireless systems design and the associated challenges.

Detailed Abstract:
Advances in wireless technology are being driven primarily by the transformation of what has been largely for a medium for supporting voice telephony into a medium for supporting other services, such as the transmission of video, images, text, and data. This, in turn, is enabling wireless technology applications to become pervasive, across a wide array of product domains like life sciences, consumer, industrial, telecommunications etc. The pervasiveness of wireless applications makes it imperative for the design community to take a systems engineering approach. The aim of this tutorial is to provide a strong theoretical background necessary for wireless system design. It helps to develop a detailed technical knowledge of current practice in wireless systems and networks. It addresses the systems engineering challenges, associated with design and development of wireless systems for multiple applications / domains, with an in-depth discussion through relevant design case studies.

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Integrated Chip Quality For Automotive Applications

Raghavendra Dattatraya; **Jagadeesh Nallagatla**; and **Poornima Prahlada** (NXP Semiconductors)

Coordinating Presenter: Raghavendra Dattatraya

Summary:

Automotive products need very high accuracy as the margin for error in their control systems and sensors etc. is almost nil. Testability and the coverage targets always aim to hit 100%, though the cost incurred is big. The Design For Test (DFT) covers the fault modeling and generation of test procedures to cover various physical and electrical defects. However achieving quality and yield, demands considerable effort in design implementation. Issues such as considering various process corners, environmental conditions, process limitations etc. need to be accounted during design implementation to achieve higher yield and defect free ICs. This tutorial introduces various quality measures required for ICs used in automotive applications, impact of higher integration, choice of technology node, second order effects cum Design For Manufacturability (DFM), issues associated with deep submicron technology nodes, mapping the challenges into respective domain (physical, performance etc) and the design methodologies needed to achieve higher yield.

Tutorial outline:

- *Introduction*
- *Overview on IC development flow*
- *Quality requirements for ICs used in automotive applications*
- *Overview on trends in technology node development*
- *Transistor second-order effects and their impact on performance and quality of IC*
- *Overview on lithography used in IC manufacturing and challenges involved*
- *Demonstration of Multi Mode Multi Corner based IC design implementation*
- *Demonstration of Lithographical aware IC implementation and checks*
- *Demonstration of Low power implementation*
- *Demonstration of meeting DFM compliance in IC implementation*

Presenters' Biography

Jagadeesh Venkata Nallagatla: is working as Senior Technical Leader in Business Unit Automotive / Business Line Car Entertainment Solutions in NXP Semiconductors India Pvt Ltd. He has been with NXP / Philips for 3.5 years. In his role, he is involved in netlist to gds2 activities for NXP Automotive products. Prior to this role, he was involved in the physical design activities for DTV SoCs, Set Top Box SoC's and SoC's for various business units inside NXP.

He is pursuing M. Sc. In VLSI System Design, from Coventry University (UK) through M S Ramaiah School Of Advanced Studies, Bangalore. He has 10 years of total industrial experience during which he has also worked for Connexant Systems, Qualcore Logic Limited, etc.

Raghavendra H Dattatraya is working as the Senior Technical Leader in Business Unit Automotive / Business Line Car Entertainment Solutions in NXP Semiconductors India Pvt Ltd. He has been with NXP / Philips for 4.5 years. In his role, he is involved in the development of SoC's for NXP Automotive products. Prior to this role, he was involved in the physical design activities for cell phone processors SoC's, Cordless Soc's ,DTV SoCs,Set Top Box SoC's and SoC's for various business units inside NXP.

He has B.Tech in Electronics and Communications from University Visvesvaraya College of Engineering .He has 11 years of total industrial experience during which he has also worked for IBM Microelectronics.

Poornima Kittur Prahlada is working as Technical Leader in Business Unit Automotive / Business Line Car Entertainment Solutions in NXP Semiconductors India Pvt Ltd. She has been with NXP for 3.5 years. In her role, she is involved in the development of SoC's for NXP Automotive products. Prior to this role, she was involved in the physical design activities of Set Top Box SoC's , DTV SoCs and SoC's for various business units inside NXP.

She has B.Tech in Electical and Electronics from JNNCE Shimoga . She has 9 years of total industrial experience during which she has also worked for Freescale Semiconductors and Wipro Technologies.

Design and Verification with SystemC

Bhanu Kapoor (Mimasic), **Prapanna Tiwari** (Synopsys), **Shireesh Verma** (Conexant),
and **Rahul Joshi** (Chip Design Pvt. Ltd., Gurgaon)

Coordinating Presenter: Bhanu Kapoor

"Design and Verification with SystemC" provides a comprehensive introduction to the powerful modeling capabilities of the SystemC language using a rich set of examples and techniques used with SystemC. SystemC is a naturally object-oriented language that allows designers to use familiar hardware concepts such as modules and interfaces to model their design at high and intermediate levels of abstraction. A gentle introduction to the object-oriented programming paradigm is provided using the C++ language. We then get attendees up to speed with SystemC programming concepts such as data types, modules and hierarchies, processes and time, interfaces and channels, adapters, bus modeling, and transaction-level modeling using Open Source SystemC Simulator. All of this is geared to enable smooth transition to design and verification with SystemC. We also provide an overview of available software tools that work with SystemC to aid design and verification process.

Overview

- **Overview of SystemC**

✓ C++ background for System
✓ Introduction to SystemC RTL
✓ Modeling Synchronous Logic with SystemC
✓ Writing Testbenches with SystemC
✓ Introduction to the SystemC Simulator
  - o Setting up SystemC Simulator
  - o Creating a small arithmetic module
  - o Simulating arithmetic module for validation

- **Modeling Beyond RTL**

✓ Processes in SystemC
✓ Ports, Interfaces, and Channels
✓ Notion of Time and Concurrency
✓ Basic Channels and Interfaces
✓ Packet-based Verification in Networking
  - o Packet Generation
  - o Driving Packets to Ports
  - o Error Injection

- **Transaction-Level Modeling (TLM) Methodology**

✓ Abstraction models
✓ TLM-Based Methodology
✓ An Introduction to TLM2

Presenters' Biography

Dr. Bhanu Kapoor is the founder, president, and owner at Mimasic, a consulting services company in the area of digital low power design and verification. He started his career with Texas Instruments where he played various technical roles (1987-99) at TI's DSP R&D Center. He has played leading technology development roles in EDA startups ArchPro (now Synopsys), Atrenta, and Verisity (now Cadence). He is an expert in the area of low power design and verification. He is the lead inventor on 6 US patents in the area of low power design and verification and has over 40 publications in various IEEE/ACM conferences and journals. Bhanu graduated from the Indian Institute of Technology (IITK) in 1987 with a degree in Electrical Engineering. He has received M.S. (1990) and Ph.D. (1994) degrees in Computer Science from SMU, Dallas.

Prapanna Tiwari graduated in 2001 with a B.Tech. Degree in Computer Science. Spent 3.5 years in TI working on silicon reliability, power integrity, IR drop analysis and decap estimation. In 2005, he joined ArchPro Design Automation as one of the early employees developing dynamic and static low power verification solutions. He later joined the Application Engineering team to work