A Simulation based study & analysis of Double Gate Tunnel FET Performance for Low Standby Power Applications

Nayan B Patel[1] **Santanu Mahapatra**[2]

Abstract

The conventional metal oxide semiconductor field effect transistor (MOSFET) may not be suitable for future low standby power (LSTP) applications due to its high off-state current as the sub-threshold swing is theoretically limited to 60mV/decade. Tunnel field effect transistor (TFET) based on gate controlled band to band tunneling has attracted attention for such applications due to its extremely small sub-threshold swing (much less than 60mV/decade). This paper takes a simulation approach to gain some insight into its electrostatics and the carrier transport mechanism. Using 2D device simulations, a thorough study and analysis of the electrical parameters of the planar double gate TFET is performed. Due to excellent sub-threshold characteristics and a reverse biased structure, it offers orders of magnitude less leakage current compared to the conventional MOSFET. In this work, it is shown that the device can be scaled down to channel lengths as small as 30 nm without affecting its performance. Also, it is observed that the bulk region of the device plays a major role in determining the sub-threshold characteristics of the device and considerable improvement in performance (in terms of I_{ON}/I_{OFF} ratio) can be achieved if the thickness of the device is reduced. An I_{ON}/I_{OFF} ratio of $2x10^{12}$ and a minimum point sub-threshold swing of 22mV/decade is obtained.

Keywords: Sub-threshold Swing, Tunnel Transistor, Band to band tunneling

1. Introduction

Relentless downscaling of the CMOS technology has led to immense improvements in its performance. However, the switching characteristics of the MOSFET have degraded considerably over the years as a result of scaling. The sub-threshold swing (S) is a very important parameter for any switch. S is defined as the amount of gate voltage needed to change the drain current by 1 decade. It indicates how effectively the MOSFET can be switched OFF by decreasing the gate voltage below threshold voltage (V_{TH}). It also determines the off state current, I_{OFF} (at $V_{GS} = 0$), of the switch. For an ideal switch, S is equal to zero and this leads to a zero off-state current. (Figure. 1)

The MOSFET uses the drift-diffusion mode of carrier transport, and the drain current in the sub-threshold region ($V_{GS} < V_{TH}$) of operation is given by [1],

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Multilevel Pyramidically Wound Symmetric Spiral Inductor

Genemala Haobijam[•] and Roy Paily[•]

Abstract

In this paper a new multilevel pyramidically wound symmetric spiral (MPSS) inductor structure is presented. The proposed structure achieves higher inductance to area ratio and its symmetrical nature eliminates the need of a pair of planar inductors for differential circuit implementation. The chip area occupied by the inductor is reduced significantly. The performance of MPSS inductor is evaluated by the design of 8 nH and 23 nH inductors. An MPSS 8 nH inductor, designed in a 0.35 µm technology reduces the area by 65% to 95% as compared to its equivalent conventional asymmetric and symmetric inductors of same metal width and number of turns varying from 2 to 6. When compared to its equivalent pair of 4 nH planar inductors for differential circuit implementation, the MPSS inductor reduces the area by 71% to 94% and quality factor increases by 20%. The self resonating frequency of the MPSS structure is higher by 55% than conventional stack structure. Performance is characterized using a 3D Electromagnetic simulator. With MPSS inductor, the cost and size of RF IC's will be reduced significantly.

Keywords: *Multilevel symmetric spiral, RF IC's, Quality factor, EM simulation, Monolithic inductor.*

1. Introduction

Monolithic inductors are one of the important passive components of various radio frequency integrated circuits (RF IC's) that determines the overall performance and cost. The overall area occupied by the inductors is very large as compared to area occupied by active devices and hence increases the production cost. To realize low-cost RF CMOS technology, the performance of the passives must be traded off with the cost of incorporating them on chip [1]. In integrated circuits like amplifiers, mixers, oscillators etc. the differential topology is mostly adopted because it is less sensitive to noise and interference. Generally, a planar inductor is asymmetric and hence for differential circuit implementation, a pair of spiral inductors is used with their inner loops connected together as shown in Fig. 1. The design parameters of a monolithic inductor includes the spiral track width (W), spiral track spacing (S), outer diameter (D_{out}) and inner diameter (D_{in}) and number of turns as indicated in the figure. Since the currents flow in opposite direction in the two inductors, there must be enough spacing between them to minimize electromagnetic coupling.

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FLOATING GATE INTERFERENCES ON V_{TH} DISTRIBUTION IN EIGHT LEVEL HIGH DENSITY FLASH MEMORY

B Vikas[1] ,R P Paily[2] and Yajun Ha[3]

Abstract

As the dimensions are shrinking, eight level NAND flash memory goes into critical issues like floating gate interferences and process variations. These problems widen the targeted V_{th} distribution of each state and adversely affect the performance. To verify the feasibility of a design, estimations of the process variation effects and inter-cell coupling ratios are essential. Therefore, we have computed various stray capacitances and coupling ratios in an array of cells for 350nm to 90nm technology nodes. From these values, one can calculate how much the V_{th} distribution of a particular cell is affected by the interferences from adjacent cell programming. The effect of different dielectric spacers between the control lines and bit lines are also investigated. Even with an oxide spacer for 90nm design rule, the worst case floating gate shift obtained was as high as 0.19V.

Keywords**:** *NAND Flash, Multi Level Cells, Floating gate interference, Coupling ratios, V_{th} distribution, Process variations, Simultaneous programming.*

1. Introduction

Memories are essential for preserving critical information in a non-volatile condition. Almost 90% of non-volatile memory is made up of floating gate transistors. Semiconductor memories are becoming more demanding due to its high speed, low power, less weight and portability in PDA, Mobile and other applications. Among NAND and NOR architectures, NAND is more appropriate for file storage applications due to its high density and high throughput. In the NAND structure, a series of floating gate transistors are connected between the bit line and ground line. This organization allows the elimination of all contacts to ground line and thus reducing the area by 40% compared to NOR architecture [1]. The programmability is achieved by different mechanism like channel hot electron tunneling or FN-tunneling [2] of V_{th} (threshold voltage of the floating gate transistor) changes of transistor by the injection of electrons into floating gate transistor. Similarly, by removing the charges from the FG (floating gate) V_{th} can be restored. Supply voltages needed for programming like V_{pass} [2] (V_{pass} is the voltage given to the unselected word lines in the selected block) and V_{pgm}

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An Algorithm for Resistance Extraction and Current Density Profiling of Lateral Power MOSFETs

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Abstract

This paper puts forward a novel hierarchical approach for solving the problem of resistance extraction and current density profiling of lateral power MOSFETs primarily used in switching voltage regulators. In the absence of standard resistance extraction tools targeted to power arrays, the analysis of such power arrays becomes quite difficult. Iterations while designing the power arrays makes the design slow. Commercial extraction tools usually provide inaccurate and inconsistent results. The proposed algorithm exploits the inherent geometric symmetry present in the layout of Power MOSFETs using a Finite Element Method (FEM) based approach integrated with hierarchical bottom up combination techniques. Finally, a backtracking approach is also proposed that would generate a current density profile of the layout. This uses a top-down algorithm combined with efficient storage techniques.

Keywords: Resistance Extraction, Hierarchical Analysis, Lateral Power MOSFETs.

1. Introduction

Power Management has become a very important and challenging aspect of modern day battery operated integrated circuits and systems like PDAs, mobile phones, MPEG players etc. A major challenge facing the designers of such devices is to improve the battery life. These devices use Power switches which need to be designed optimally with minimum RdsON and parasitic capacitance to ensure high power efficiency.

MOS switches typically have high values of W/L, which are broken up into an array of devices with a smaller W/L connected through an arrangement of interconnects and vias. Interconnect resistance starts dominating beyond a certain array size and the minimum feature size of the process. MOS transistors need to have low resistance in their on state (RdsON) to improve their efficiency. It also becomes very important to carry out the voltage and current density profiling to locate the presence of thermal hotspots if any. The creation of such hotspots may result in the failure of the chip.

Over the past three decades, a lot of research has been done in the field of parasitic resistance extraction of ICs. The Boundary Element Method was applied for two dimensional resistance simulation which reduces the number of nodes [1,2]. However the matrices obtained are not sparse in nature. Also the analytical nature of the approach makes it difficult to work on irregular array structures. Calculation of admittance matrix and resistance network has also been applied to solving the extraction problem to IC's

An Error Comparison Scheme for Design Rule Checking Flows

Dibyendu Goswami[1], Swami Gangadharan[2]

1. ABSTRACT

In deep sub-micron regime, Design Rule Checking (DRC) has become enormously complex. The number of design rules to be checked on a design has grown multifold, which leads to a huge run time for the physical verification tools. In order to cope with ever increasing demand from customers to provide faster and more accurate layout verification solutions, a verification engineer tries to explore different and newer tools that would give the run-time and accuracy improvement that is sought. But, shifting to a different layout verification tool is not a simple task, as it requires a thorough validation of the new tool with respect to the POR (Plan Of Record) tool. There are a large number of DRCs checked on a design and he/she has to make sure that there is no discrepancy between the two tools in terms of design rule checking. When an "error found, error missed" discrepancy occurs, it's the verification engineer's job to find out why the error is missed by one tool, but detected by another tool. This work becomes even more cumbersome when the input database size is very large since locating the place where the mismatch occurs may take a lot of time to figure out.

In this paper, we describe a novel methodology that enables the accurate comparison of DRC errors generated by one tool and the DRC errors generated by another tool. An automated flow that can generate DRC error databases using two different layout verification tools and subsequently compare the DRC errors according to the methodology described herein has also been developed. This flow can also be used to validate a newer version of the verification tool with respect to the POR version. Lastly, it can also be used to compare two different versions of a runset (rules deck) written for the same tool.

Key Words:
Design Rule Check (DRC), Hercules, Calibre, Physical/Layout Verification, runset.

2. INTRODUCTION

IC fabrication process becomes enormously complicated in the sub-wavelength regime as the feature sizes reach a fraction of the wavelength of the light being used to fabricate them. This increased process complexity contributes to more stringent design rules. EDA (Electronic Design Automation) vendors strive to come up with newer versions of verification tools and sometimes with brand new tools so that these most stringent rules can be checked in a very simplistic manner leading to an improvement in total throughput and accuracy. In order to shift to a new version of a verification tool, layout verification engineer must ensure that there is no mismatch with respect to the POR version of the tool in terms of DRC errors reported by both of them. Similarly when a brand new tool is adopted there must be some co-relation established for each DRC error reported by this tool versus the POR tool and vice versa. Our auto comparison

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Delay Clock Methodology for Timing-Performance Improvement of Designs on FPGAs

K. Vinay, R.D. Singh, S. Maleka, V. Kamakoti[1] and Anirban Rahut[2]

Abstract

This paper presents a technique that improves the maximum operational frequency of a pipelined design using the Delay Clock Methodology (DCM).. This paper deals with generic flip-flop-based pipelines that have branches and feedback paths. To improve the confidence of the correctness of execution of the design, a new confidence metric, namely, the K-ALOOFNESS is introduced. The technique is further fine-tuned for Field Programmable Gate Arrays (FPGAs). The effectiveness of the proposed concept is verified by applying the same on reasonably complex FPGA-based designs.

Keywords: Delay Clock Methodology, Clock Phases, Wave Pipelining, FPGAs, Constraint Solving

1. Introduction

Most of the modern designs are pipelined. The *maximum stage* delay of the pipeline determines the operational frequency. Several attempts are reported in the literature to circumvent this problem. Multi-cycle paths and latch-based time borrowing techniques are reported in Sakallah, Mudge, and O. A. Olukotun (1992)} that improves the clock frequency. The above techniques result in *wave-pipelining* as described in Burleson, Ciesielski, Klass, and W. Liu (1998) and Joy and J. Ciesielski (1993), wherein, two or more consecutive data sets are in process in a single combinational stage of the pipeline at any instant of time.

Figure 1 describes the Delay Clock Methodology (DCM) technique for improving performance. In figure 1, C_1 and C_2 are combinational blocks with delays 30 *ns* and 20 *ns* respectively. In a normal scenario, the time period of the clock controlling the pipeline would be 30 *ns*. Note that, a delay (skew) of 5 *ns* is introduced to the clock feeding the flip-flop FF_b. This helps the pipeline to operate with a clock whose frequency is 25 *ns* as follows: The first set of data (refer to the timing diagrams of the clocks *CLK1*, *CLK2* and *CLK3* driving FF_a, FF_b and FF_c respectively in Figure 1) is driven into C_1 by FF_a at time *p*. It reaches FF_b at time *u*, coinciding with the positive edge of *CLK2* driving FF_b

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Layout-Aware ILS Design Technique

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Abstract

The Illinois Scan Architecture (ILS) consists of several scan path segments and is useful in reducing test application time and test data volume required to test today's high density VLSI circuits. However, to achieve high fault coverage with ILS architecture one requires judicious grouping and ordering of scan flip-flops for selecting these segments. This may also increase the wiring complexity and cost of the scan chain, as the physical locations of the flip-flops on silicon are determined at an early design stage before scan insertion. In this paper, we propose a scheme of layout-aware as well as coverage-driven ILS design. The partitioning of the flip-flops into ILS segments is determined by their geometric locations, whereas the set of the flip-flops to be placed in parallel is determined by the minimum incompatibility relations among the corresponding bits of a test set, to enhance fault coverage in broadcast mode. This consequently, reduces the number of test patterns required in serial mode. The proposed methodology reduces test application time significantly, and at the same time, achieves high fault coverage. Switching power dissipation in the scan cells can be reduced by further reordering of groups in the segments. The method also allows the user to choose the number of segments required to achieve desired wiring cost, test application time, and fault coverage. Experimental results on various benchmark circuits demonstrate the efficacy and versatility of the proposed method.

1. Introduction

The controllability and observability of a digital circuit can be increased by various well-known design-for-testability (*DFT*) techniques. Among them, the serial full scan style is widely used, which transforms a sequential circuit to its combinational parts in test mode. Although this method reduces the cost of test generation and provides high fault coverage, the test application time and power dissipation in test mode become significantly high because of the inherent serial nature of the scan path. It also increases test data volume. As most of the systems now consist of thousands of flip-flops, memory requirement for storing test data in automatic test equipment (*ATE*), as well the test time becomes unacceptably high. An *ATE* with a large storage device slows down its memory access time and the test clock frequency.

Among the existing methods that are used to tackle the problem of reducing the test application time, one approach is to configure the scan elements into multiple scan chains [1, 2]. However, this increases the number of scan-in pins (*SIP*) and scan-out pins (*SOP*) during test and does not reduce the test data volume. This technique also requires additional *ATE* channels to deliver the test patterns and to retrieve the corresponding test responses.

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Compression-Power Trade-off in Dictionary based Test Data Compression

Chandan Giri[1], Nikhil Reddy Cheruku[2] and Santanu Chattopadhyay[3]

Abstract

Test data compression and scan chain transition reduction are two fundamental problems in testing large system-on-chip designs with power limitations. While most of the works reported aims one of these two objectives, a joint approach to handle both is very much desirable. In this direction, some of the reported works does a compromise in either the compression or the transitions. This paper presents the test engineers with the total available trade-off between the compression ratio and scan-in power consumption in dictionary based test data compression. A suitable point on the trade-off graph can then be selected to satisfy the test requirements.

I. Introduction

Several Intellectual Property (IP) cores can be integrated in a single chip in current state-of-the-art design paradigm called System-On-Chip (SOC). This complex system challenges test engineers to have a power efficient strategy along with reduced testing time. For increasing number of cores, handling large volume of test data is a critical problem as it affects directly the Test Application Time (TAT). To solve this problem researchers have come up with different test data compression techniques. Compressed test data are sent from Automated Test Equipment (ATE) to the Circuit Under Test (CUT) through Test Access Mechanism (TAM). Another important issue in testing that has come up recently is about power minimization during testing. This is required as most of the chips today come up with a power budget. Thus, excessive power dissipation during test and the associated heat generated may cause permanent damage to the chip. Various strategies have been provided in the literature to compress the test data to reduce test application time. Various strategies have also been given to reduce the test power.

Reduction in volume of test data [1-5] and test power minimization [6,7] has been previously treated as two separate design objectives. Proposed methods like [8-12] starts from a set of test cubes, maps the don't cares to 0s or 1s and compress the resulting test set using different encoding techniques. It shows that significant reduction in test data volume is achieved along with a reduction in the transition count, therefore reducing test power consumption. In [8] don't cares are filled with 0s and Golomb encoding method is used to compress the test data. In [9] authors used run length encoding technique followed by Huffman coding to reduce test data volume and simultaneously it reduces the scan-in power also. In [10] authors showed combination of symmetric coding scheme and a weighted

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Fault Diagnosis of Reversible Circuits

Susanta Chakraborty [1], Bikromadittya Mondal [2], Bhargab B Bhattacharya [3]

Abstract

Reversible logic plays a significant role in quantum computing and nanotechnology. The paper proposes a design of MISA with reversible gates and addresses that n repetition of the last test vector is required for detecting all single, multiple and partial missing gate faults. The results on reversible benchmark circuit show that it requires n repetitions, which is a significant reduction compared to n^2 repetition of classical circuits.

Keywords: Reversible gate, quantum computing, missing gate fault, MISA.

1. Introduction

Reversible logic has a vital role in low power CMOS quantum computing, nanotechnology and optical computing. Quantum computation can solve exponentially hard problems in polynomial time[9]. Quantum circuit is represented by a qubit. The unit of quantum information is called a *qubit*. A qubit can be in a zero or a one state. Our approach based on the trapped-ion technology which uses the certain spin and vibrational modes of electrically charged ions as the qubit representation. Most gates used in classical digital design are not reversible. Controlled –NOT(CNOT) gates proposed by Feynman[6], Toffoli gates[5], and Fredkin[7] gates are well known reversible gates that needed to design reversible circuits. Proposed fault diagnosis method can detect single missing gate, multiple missing gate and partial missing gate faults[1] in reversible circuits.

A pseudorandom test pattern is applied to the CUT. Test inputs are supplied to the CUT and the corresponding test responses are accumulated into a signature by multi input signature analyzer (MISA) of reversible gates. If the signature is correct, the CUT is assumed to be fault free. If the signature is erroneous the same input are applied to the CUT and the corresponding outputs of the CUT are again accumulated in a signature. But now we monitor the output of the MISA. A first erroneous bit of this sequence is detected. In the last step the last test input is submitted n times to the CUT, where n is the number of inputs in the CUT.

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Design of Synchronous Buck Converter Employing an Adaptive Zero Voltage Switching for Ultra Low Power Systems

Sandeep Mehra[1] and Bharadwaj Amrutur[1]

Abstract

We investigate the design of a DC-DC buck converter for ultra low power applications like the sensors nodes of a Wireless Sensor Network. A Pulse Frequency Modulated (PFM) controller with Zero Voltage Switching (ZVS) is typically employed for very low load currents of less than 50mA. We propose an adaptive technique to implement Zero Voltage Switching (ZVS) and Inductor current sensing under dynamic load conditions, using clocked comparators. The low power comparators along with adaptive timing control minimize losses to improve the efficiency of the converter to 74% which is 10% higher than the previously reported discontinuous mode buck converters, Stratakos (1997), Zhou and Rincón-Mora (2006), Musunuri, et. al (2005), of less than 1mW range.

Keywords: DC-DC Converter, Low Power

1. Introduction

Recently, new ultra low power applications like wireless sensor networks have emerged, which consume very low currents of less than *20mA*, yet need a regulated efficient supply. Design of efficient DC-DC switching converters for such low currents will be challenge as the previously neglected loss mechanisms in controllers like the comparators and the mis-timing of the switching waveforms become very important. The basic approach followed in most of previous techniques (*Zhou and Rincón-Mora (2006), Long (2006), Dancy et. al (2000)*) is to employ large Filter Inductor(L_f) to ensure continuous mode operation. The drawback of this technique is that it is designed to obtain good efficiency for a particular load range and if the load decreases below this range, the converter moves into a discontinuous mode thereby introducing losses.

Stratakos(1997) employs PFM (pulse frequency modulation) technique for low load currents. But this technique suffers from low efficiency due to static currents in the comparators as well their sluggish response.

The authors in *Long et. al (2006)* employ clocked comparators, but the sampling clock operates at frequencies in GHz range. The overhead of using fixed high frequency clocks is not significant in large load conditions, but for low load

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A 2.4 GHz low-voltage CMOS Low Noise Amplifier with 32 dB gain

Anuradha Ray[1] **and Chetan Parikh**[2]

Abstract

This paper proposes a topology for a CMOS low noise amplifier (LNA) at 2.4 GHz. The basic architecture consists of an inverter followed by a common-gate (CG) amplifier. Compared to other existing architectures, the new topology provides a more stable dc biasing scheme, has a higher gain and a comparable IIP3. Spice results show that for a supply voltage of 1.2 V, the amplifier gives a voltage gain of 32 dB, a noise figure of 3.4 dB, and consumes a dc power of 3.5 mW.

Keywords: Low-noise amplifier, CMOS, RF, LNA

1. INTRODUCTION

The low-noise amplifier (LNA) is one of the most important building blocks in the front-end of wireless communication systems. It determines the noise performance of the overall system, as it is the first block after the antenna. In the last few years, LNA's are being increasingly designed with MOS transistors (in place of the traditional bipolar transistors) due to their low cost, possibilities of high levels of integration, and their increasing cut-off frequencies with scaling technologies. In recent years, much research has been done on CMOS LNA design, from topology investigation [1-2], to new ideas on achieving low power consumption [3-5], low noise figure and high gain [6], less chip area [7], and lower supply voltages [8-9].

In this paper, we propose a new design of a single-ended CMOS LNA for 2.4 GHz applications. The basic topology is that of a folded cascode amplifier [9]; but instead of an NMOS driver transistor, we use a CMOS inverter [3]; further, we separate the PMOS and NMOS transistors of the inverter, as will be discussed in the Sec. 2, to stabilize the bias point, and to increase the voltage headroom. Simulation results show that compared to other existing architectures, this new architecture consumes slightly less power, provides a more stable dc biasing scheme, has a slightly higher gain and comparable IIP3 and –1 dB compression-point figures.

The paper is organized as follows. Section 2 describes the proposed new architecture circuit and explains its functionality. Simulation results are presented in Section 3 and the paper is summarized in Section 4.

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Design and implementation of a 14-bit 200 MSPS Current Steering DAC using Gm/Id method

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Abstract

In the literature, square law model is used for the design of transistors in the current steering DAC. This model is not applicable when the transistors operate in moderate inversion region. However, minimization of current cell area is achieved at the cost of overdrive voltage. Limited supply voltage and large output swing of DAC may force some of the transistors in the cascode current cell to operate in moderate inversion region. To overcome this limitation, Gm/Id synthesis procedure is proposed in this paper for the design of current steering DAC. Its effectiveness is studied by designing a 14-bit, 200 MSPS Current Steering DAC in TSMC 0.35µm technology. From the design and simulation results, it is observed that the current cell synthesized using Gm/Id method results in 33% less current cell area than that using the general design method and this is achieved without any compromise on speed. It is found that INL and DNL are less than 0.45 LSB and 0.25 LSB respectively.

Keywords: *Current steering, DAC, Gm/Id*

1 Introduction

High speed and high resolution DACs are required for a variety of communication subsystems such as cellular base stations, cable modems and video codecs. Current steering DACs (CSDACs) are commonly used for such high speed applications. A number of CSDACs have been proposed and are reported in the literature. Details of a 10 bit CSDAC operating at an update rate of one GSPS is reported in [1]. CSDACs with resolution of 12 – 14 bits and operating at few hundreds of Mega Samples per second are reported in [2], [3], and [4]. Almost all of these works, use square law model for the design of transistors, and give accurate results when dynamic output impedance is small.

If high dynamic output impedance and high resolution of the order of 12 - 14 bits are simultaneously required, it is necessary to include cascode transistors [5] to the basic current cell. With the limited supply voltage, it is impossible to maintain all the transistors in the current cell in saturation condition. This makes the square law based Vdsat method [1], [2], [3], [4] to be inaccurate. To overcome this problem, the Gm/Id method is adopted for the design of transistors in the current cells of CSDAC in this paper. The Gm/Id method proposed in [6], [7], is accurate for transistors operating in any region

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Game Theory and its Application to VLSI Physical Design

Parthasarathi Dasgupta[1]

Abstract

VLSI Physical design problems typically involve solving some of the hardest problems of combinatorial optimization. Complex process technologies in the deep submicron regime and rapidly reducing feature sizes have augmented the hardness with increasing number of objectives and constraints. Most of these objectives appear to be conflicting in nature. Game theoretic modeling plays a useful role in solving such multi-objective problems. It relies on features of rationality, coalition formation, competition, and equilibrium. The outcome is typically a solution that is the best for a player with respect to every other player's objectives and decisions. Each player has an associated payoff function, measuring its expected utility in the game. The goal is to find a solution that is the best (or optimum) for all the players. A game is said to reach equilibrium when the combination of strategies of all the players has the best possible payoff for all the players. Introduced by Von Neumann in early twentieth century, Game Theory was originally a subject of economists, social scientists, and mathematicians. It has recently found applications in Electronic markets, Computer networking and other fields of Computer Science including formulation and solving the hard problems of the VLSI Physical Design.

Keywords: VLSI Physical design, Interconnect routing, Game Theory

1. Introduction

The general idea of a game between several players is to start from a given point and to proceed with a sequence of moves by the different players. At each instance of the game, a player has to choose a possible action from a set of several possibilities depending on the previous actions by different players. A player may even apply a random move, such as throwing a die or shuffling a deck of cards. Formally, a *game* is a structured or semi-structured activity, usually done for enjoyment. Key components of games are goals, rules, challenge, and interactivity. In *game theory*, the word *game*, used in the metaphoric sense, typically refers to a sequence of interactions between several players. The outcome of a game depends on the sequence of actions or moves by the players. The pioneering works by von Neumann in 1928 [Neumann 1928] and Nash in 1950 [Nash 1950] form the basis of Game Theory. Game Theory has been extensively studied in the past from the viewpoint of mathematics and economics, and several applications proposed [Osborne and Rubinstein 1994]. However, very recently, it has found enormous applications in several other areas such as the design of electronic markets, computer networking,

Low-power High Slew-rate Adaptive Biasing Circuit for CMOS Amplifiers

Narayana Rao[1] and Chetan Parikh[2]

Abstract

In this paper, an adaptive-bias circuit is proposed for CMOS amplifiers. The circuit differs from previous adaptive-bias circuits in that here, a single circuit provides both static and dynamic biases, thus achieving a further reduction in power. The proposed circuit requires a very low standby power and provides a high slew rate for large differential input signals. Compared to a fixed-bias amplifier, the adaptive-biased amplifier has nearly seven times higher slew-rate, with the same quiescent power dissipation. If the design is optimized to achieve the same slew-rate, then a reduction of more than 70% in the quiescent power is achieved.

Keywords: CMOS amplifier, adaptive bias, high slew-rate, low power

1. INTRODUCTION

Proliferation of battery-operated systems in computation, communication and biomedical applications has created a lot of activity in the design of low power integrated circuits. In CMOS digital circuits, static power dissipation is very low and dynamic power dissipation can be reduced by supply voltage scaling. On the other hand, analog circuits typically have continuous standby power dissipation. The main causes of quiescent power consumption in op-amp based analog circuits are the current sources inside amplifiers. Reducing biasing currents severely limits the large-signal transient performance (e.g. slew-rate), and the gain-bandwidth.

In the literature, CMOS adaptive biasing circuits have been proposed to give low standby power without reducing driving capability [1-3]. In [1] and [2], the biasing current is the sum of a constant current source and an input dependent current source. The input dependent current is proportional to the difference of currents in the input differential pair. In [3], two bias stages are used (static bias and dynamic bias). In [2], two additional current sources are used in the biasing circuit to provide the quiescent bias current. The disadvantage of these techniques is that they draw additional current from the supply, consequently causing additional static power dissipation.

In this paper, a single, fully adaptive, biasing circuit is proposed, which provides a small quiescent current and a large dynamic current without any need of additional current sources or a static biasing circuit.

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Design of high performance current steering DAC using pattern search algorithm

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Abstract

In this paper, the pattern search algorithm is adopted to choose the optimum size for the transistors in the current cell of a DAC and their gate voltages in order to obtain better static and dynamic performance at circuit level. Moreover, the double cascode structure is proposed for the current cell to increase the dynamic output impedance for high resolution DAC. Efficacy of these techniques are studied by designing a 14-bit, 200 MSPS Current Steering DAC using TSMC 0.35µm technology. The proposed DAC is segmented into 8 MSB thermometer and 6 LSB binary bits. For a dynamic output impedance of about $10^{15}\Omega$, the double cascode structure designed using the optimization algorithm requires about 60 times less area than the single cascode cell structure. From the simulation results, it is found that the INL, DNL and SFDR at 2 MHz for the DAC with double cascode structure are 0.43 LSB, 0.25 LSB and 76 dB respectively.

Key words: *current steering ,DAC ,pattern search algorithm*

1 Introduction:

The advancements in the silicon process technology enable the implementation of a complete system consisting of both digital and analog blocks including D/A and A/D converters on a single chip. High performance digital-to-analog (D/A) converters find applications in the areas of video, wireless communication and broad band communication, e.g., HDTV and GSM. Such applications require DACs to be capable of handling data at speeds of several tens or hundreds of Mega Samples/sec, with data resolution of the order of 10–14 bits. The design of current cells with minimum size and with good dynamic as well as static performance is one of the challenges. Because of the speed and lower cost, CMOS current-steering D/A converters are ideal for such applications. In the literature, circuit level design of DAC meeting the static performance and minimizing settling time is reported [1] [2]. It is reported that for a good dynamic performance, DAC requires high output impedance [3]. In this paper, a procedure for the design of current steering segmented DAC is proposed using pattern search algorithm.

The organization of the paper is as follows: An overview of a current steering DAC and different current cell topologies is given in section 2. Design equations for both static and dynamic performance of DAC with and without cascode cells and extension of these equations for current cell with double

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Crosstalk Noise Analysis Tool and Development of an Automated Spice Correlation Suite to Enable Accuracy Validation

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Abstract--*As process geometries are shrinking, width of the metal layer is continuously decreasing, height of the layer and wire lengths are increasing, thereby increasing the effect of coupling capacitances. Coupling induced crosstalk may induce unwanted noise on coupled signal nets resulting in functional failure and performance degradation and becomes a significant limitation in achieving first pass silicon success. At the same time the complexity of noise analysis has significantly increased due to factors such as driver weakening, IR drop, voltage scaling and variations in manufacturing processes. Therefore validating the capabilities and verifying the analysis of a crosstalk analysis tool for current and future process nodes is very critical for efficient and accurate signoff analysis. The modeling of the cell itself needs to be accurate and comprehensive. Accurate analysis of special cells without additional library requirements. An efficient propagation methodology and identifying true violation sources to reduce design cycle time and pessimism. A complete hierarchical solution is useful to analyze large designs. Accuracy, runtime and CPU resources for characterization, considering, one-time library characterization v/s on-the-fly for the required design cells. The objective of the paper is to share the methodology and challenges involved in Crosstalk Noise Analysis and how the Composite Current Source (CCS) based Crosstalk Noise Analysis capability of PrimeTime SI would help us achieve many of our goals.*

Keywords--*Crosstalk, Noise Propagation, Noise Immunity Curve.*

I. Introduction

As we enter the 45nm era, comprehending and accurately determining signal integrity [5] effects is a big challenge. The impact of crosstalk effects are steadily increasing with shrinking process geometries and are often responsible for functional failures and performance degradation. This is a significant limitation in achieving first pass silicon success.

One of the important steps towards achieving first pass silicon success is the usage of an accurate crosstalk noise analysis tool which can reliably and accurately flag potential silicon failures. Validating the accuracy, capabilities, usability and reliability of a crosstalk analysis tool is very critical. As is ensuring minimal impact on design cycle time due to tool pessimism and inaccuracy. This paper shares the methodology and challenges involved in the validation of the crosstalk noise analysis capability of PrimeTime-SI [5] based on Composite Current Source (CCS) [1] modeling. There are several important aspects of evaluating a Crosstalk Noise Analysis tool for sign-off analysis. The modeling

Voltage Scalable Statistical Gate Delay Models Using Neural Networks

Bishnu Prasad Das[1], Bharadwaj Amrutur[2], H.S. Jamadagni[3]

Abstract

We propose a technique to model the delay of logic gates which captures the variability of process parameters considering intra-gate variability and is voltage scalable, using feed forward neural networks. These models can be used to efficiently generate the delay statistics across different supply conditions for use in statistical timing analysis, with very small loss of accuracy compared to SPICE based Monte-Carlo approach. The models incorporate the load and input slews as parameters and hence do away with table lookups as in the conventional approach. The model also captures temperature variation inside the chip. We demonstrate an application of the voltage scalability by using the models to do statistical timing analysis in a Dynamic Voltage Scaling framework, to obtain the optimum supply voltage for a target delay with specified statistical guarantees for some ISCAS 85 benchmark circuits.

Keywords: Intra-gate Variability, Neural network, Voltage Scalable models, statistical timing analysis

1. Introduction

On-chip variations are becoming an increasing concern in integrated circuits as transistor densities continue to increase and feature sizes continue to shrink. As device parameters such as width, length, threshold voltage of the transistor and environmental conditions such as temperature shows variability, the prediction of circuit performance, both in terms of delay and power has become a challenging task [1-3]. The conventional approach to handle this problem of variability is to use a few process corners, which capture the boundary of the process variations, to analyze the design. But such an approach is not suitable for nanometer scale devices because of the pessimistic prediction of performance spread, which inevitably leads to over design and performance loss for the typical case [2]. Hence, a new analysis paradigm based on statistical models is emerging, which attempts to incorporate the complexities of intra-die and inter-die variations in a more fine-grained way to result in less over designing and better quality results [5-9] .

Most works reported till now [5-10], only consider gate level intra-die variations. The authors in [4] show that without considering intra-gate variation, the errors can be substantial. However, to accurately model intra-gate variations, one has to consider every transistor in the gate separately, thus greatly

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Fast I/O Pad Placement in FPGAs

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Abstract

In VLSI physical design, a good placement of both the logic blocks and the input-output blocks around the boundary of the chip can ensure good quality routing of the nets. Even after proper placement of the logic blocks, a random positioning of input-output blocks can result in inefficient and bad quality routing. Here we propose a placement algorithm GENERATE_PAD_FRAME for input-output blocks, from an entirely new viewpoint. It ensures quality placement of input-output blocks along the pad frame in negligible amount of time. GENERATE_PAD_FRAME can be effectively utilized to generate equally good quality placement in FPGAs much faster. The proposed algorithm is tested on several FPGA benchmarks and the experimental results are encouraging.

1. Introduction

In the placement phase of FPGA design, exact locations of the logic blocks and the input-output blocks on the chip are determined, minimizing several criteria such as area, critical delay, total interconnects between the blocks. Besides the logic block placement, exact positioning of the input-output blocks or pads around the chip boundary, also known as *pad frame generation*, is quite significant to ensure quality placement [1, 10]. These input-output blocks on the pad frame along the chip boundary are bonded with the pins of the chip and enable the chip to communicate with the external environment. The pad frame generation primarily depends on the block-netlist information.

Our scheme first generates an ordering of I/O blocks on the pad frame and then their separation precisely on the frame by extracting information from block-netlist graph directly, without considering the exact location of the logic blocks on the chip. Placement of I/O blocks with that precise separation on the pad frame along with proper placement of logic blocks can reduce routing congestion between the I/O blocks and the logic blocks and thereby achieve good quality routing [5].

The roadmap of the paper is as follows. Section 2 describes motivation of the work. Section 3 defines the problem and other preliminaries. Section 4 discusses an overview of the proposed method, its pseudo-codes, illustrates the it with an example, and its time complexity. Section 5 presents the experimental results ands Section 6 includes the concluding remarks.

2. Motivation

Most of the heuristics for FPGA placements are based on soft-computing approaches and hence these are stochastic in nature [6, 7]. These placement

CROSSTALK ANALYSIS FOR A CMOS GATE DRIVEN COUPLED INTERCONNECTS

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Abstract: This paper deals with crosstalk analysis of a CMOS gate driven capacitively and inductively coupled interconnect. The alpha power law model of MOS - transistor is used to represent a CMOS-driver. This is combined with a transmission line based coupled RLC–model of interconnect to develop a composite model for analytical purpose. On this basis a transient analysis of crosstalk noise is carried out. Comparison of the analytical results with SPICE extracted results shows that the error involved is nominal.
Keywords- Distributed RLC Interconnect; Crosstalk Noise

1. INTRODUCTION

Wide wires are frequently encountered in global and semi-global interconnects in upper metal layers. These wires are low resistive lines that can exhibit significant inductive effects [1]. These RLC transmission lines when running parallel to each other have substantial capacitive and inductive couplings. The coupling effects are dependent on length of interconnects, distance between them, input transition time and waveform.

Predicting accurately the crosstalk waveform shape and peak noise in a driver-interconnect load system has been an important design concern since long time. Previously many researchers [2-4] have modeled crosstalk noise in distributed capacitively and inductively coupled RLC- interconnect line by representing the driving CMOS gate by a simple resistor. Agarwal et al. [3] analytically showed that a signal traveling in a coupled line system is equivalent to the superposition of two distinct modes of propagation. These modes have different propagation constants and characteristic impedances for the interconnect lines. For one of the modes (even mode) both lines switch in the same direction, while for the other (odd mode) the lines switch in opposite directions. Like other authors, Agarwal *et al.* [3] assumed the driver impedance to be a linear resistance. We show in this paper that the linearization of the transistor results in an erroneous estimation of crosstalk noise. In estimating the crosstalk effect when an equivalent linear resistor is used to model the non-linear CMOS transistors, it leads to discrepancy in results. This can be understood by noting that a transistor in a CMOS gate operates partially in the linear region and partially in the saturation region during switching. It is only in the linear region that a transistor can be accurately approximated by a resistor, where as in the saturation region, the transistor is more accurately modeled as a current source with a parallel high resistance.

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Using Hierarchy in Design Automation: The Fault Collapsing Problem

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Abstract

Although the problem of fault collapsing is not considered to be too complex, the time of collapsing faults in large circuits can be several hours or more. Large circuits are efficiently described using hierarchy, which significantly helps the architectural design, verification and physical design. We add fault collapsing to that list. We do not flatten the circuit and the collapsed fault sets computed once for sub-circuits are reused for all instances of those sub-circuits. The CPU time for collapsing faults in a flattened 128-bit array multiplier, which is about 8 hours, can be brought down to 40 seconds by using multiple levels of hierarchy. Additionally, by applying the exponential-complexity functional fault collapsing only to smaller sub-circuits, hierarchical collapsing in large circuits results in collapse ratios lower than those obtained with structural collapsing of flattened circuits. Using functional collapsing for a few small library cells, we hierarchically collapse faults in the 128-bit multiplier to sets of 480,757 equivalence and 265,824 dominance collapsed faults. In comparison, the flattened circuit collapses into 712,208 and 534,284 equivalence and dominance collapsed fault sets, respectively. We observe that the CPU time for fault collapsing for Boolean circuit by conventional programs grows as the square of the circuit size. A closer to linear time complexity can be expected for hierarchical fault collapsing.

Keywords (Index): *CAD algorithms, fault collapsing, fault modeling, testing.*

1. Introduction

Use of hierarchy allows us to solve complex automation problems like synthesis, verification and physical design. A static or structural analysis can easily benefit from hierarchy, while a dynamic analysis like simulation or test generation often flatten the hierarchy. Because fault collapsing is not dynamic, the use of hierarchy is proper choice. We show that benefits are two-fold, in reduced CPU time and in greater reduction in faults. Fault Collapsing is widely used to reduce the number of target faults for test generation and fault simulation. It has been shown [Goel (1980)] that the cost of test generation has higher than linear complexity as the number of faults increases. Hence, any technique reducing the size of the collapsed fault set would improve the performance of test development procedure for VLSI circuits. Structural fault collapsing is discussed

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Testing Droop Faults in Full Scan Circuits *

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Abstract

In deep sub-micron VLSI chips, when several transistors placed in physical proximity switch simultaneously, a substantial power supply drop, known as droop, may occur for one or more clock cycles because of concurrent load on a via of the power grid. This droop may cause cetain transistors to slow down. Such timing faults are termed as droop faults. In this paper, a model for droop faults in full scan circuits is proposed. A simple ATPG-based procedure for detecting stuck-at faults has been adapted to test droop faults. For validation of the test methodology in sequential circuits, a set of appropriate clusters of gates is selected to cover potential droop-prone regions in a circuit. Experimental results on ISCAS-89 benchmark circuits show high droop fault coverage.

Keywords: Power supply droop, transition faults, VLSI testing, full scan circuits

1. Introduction

Power supply voltage is being scaled down with the progress of technology. In nanometer design, the average current per unit area is considerably large because of the increased transistor density. Moreover, an increase in the frequency of operation and in the number of metal layers may cause a significant amount of voltage drop (both resistive and inductive) in the power grid during switching of gates [6]. For example, at 1.2V supply, a current of 0.6A flowing through a 0.4 Ω resistance causes 0.24V voltage drop. Moreover, with operational frequency in the GHz range, on-chip inductive drop *(Ldi/dt)* along the multilayer power grid can no longer be ignored. The switching delay of a logic gate may increase because of the voltage drop at the power bus contact, i.e., at the nearest M2-M3 V_{dd} via, and/or a voltage surge at the nearest M2-M3 V_{SS} via of the logic gate connected to the power distribution network [2]. Simultaneous switching of gates in the close vicinity of a M2-M3 power via may cause an excessive voltage drop at that via, termed as droop [12]. Droop at a via may lead to timing fault at one or more gates drawing power from it [13]. Modeling of droop faults and generation of test vector for such faults in combinational circuits have been reported in [13]. As in [13], we use a power grid simulator (dotted box in Fig. 1), with appropriate excitation patterns to prune and rank the list of vias according to their potential susceptibility to droop faults. Identification of droop-prone vias is based on the worst-case value of the current drawn by a via.

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A NEW APPROACH FOR TESTING OF DIGITAL MODULES IN MIXED SIGNAL VLSI CIRCUITS

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Abstract

Testing of Mixed Signal VLSI Circuits is a challenging task. Automatic testing and test pattern generation for digital circuits has been successfully solved over the last twenty years. However, if the digital blocks are embedded in between analog blocks, as in mixed signal ICs, the task of directly applying and observing test patterns and responses is not possible. Direct access to the digital blocks are to be made, so that existing tools and techniques developed for pure digital circuits can be applied. This is done either by putting boundary scan chains at digital-analog interfaces, or bringing the pins of the digital block out by multiplexing arrangements Both these techniques require design overheads in terms of area or pin count. In this work we address the above problem and try to develop a methodology that enables us to exploit the analog circuit itself to test embedded digital blocks, with minimal overheads. First, testing of digital modules in mixed signal circuits, treating the analog blocks as ideal, is addressed. Then parameter variations in the analog block are considered for developing an effective test solution. The effectiveness of the proposed method is verified by simulation of some analog benchmark circuits in SPICE.

Keywords: ATPG, DFT, Analog back trace, Sensitivity analysis

1. Introduction

Recent improvement in fabrication technology has made possible the realization of integrated circuits (ICs), containing both analog and digital functions on the same silicon. The problem of testing digital cores in these circuits is however, more complicated than that of testing purely digital cores. To test the digital block, the observability-controllability constraints imposed by the analog and conversion blocks are to be taken into account in the testing procedure. CAD tools for digital testing provides good fault coverage when the input and output

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Detection of Single Stuck-at and Bridging Faults in Cluster-based FPGA Architectures

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Abstract

This paper presents a technique for detecting single stuck-at and bridging faults in cluster-based FPGA interconnects. The same set of tests generated by a test pattern generator (TPG) detects both the faults in the FPGA circuit. In this technique, the logic elements are configured using test logic structure and the outputs of two separated logic elements are compared to detect a fault. The block under test (BUT), Test pattern Generator (TPG) and output response analyzer (ORA) are configured using some portion of FPGA circuit. The novelty of this scheme lies in the fact that the same set of test vectors can detect all the stuck-at as well as bridging faults if the test vectors are applied in a particular sequence and no extra is needed. Experimental analysis is added.

Key terms: FPGAs, stuck-at, bridging faults, BUT, Cluster based, Interconnects, BIST.

1. INTRODUCTION

Nowadays, FPGAs are widely used in many applications such as industrial automation, spacecraft and embedded systems. The FPGAs are increasingly dominating the applications where previously were exclusive territory of ASICs. Today's FPGA looks like as a system-on-chip (SOC) [20]. It has block RAMs, plenty of configurable logic and software design tools. FPGA is no longer a prototyping device. Electronic designers use FPGA because of its high flexibility in achieving multiple requirements such as high performance, no Non-Recurring-Engineering cost and fast Time-To-Market [15-16]. Note that designers, who preferred ASIC, are now using the combined FPGA-ASIC solution [22]. FPGA reprogrammability provides many interesting advantages. Unlike ASIC designs, FPGA-based implementation does not need several manufacturing process that reduces the design cycle time. The FPGA utilization decreases the overall design cost as compared to ASIC designs that need several expensive mask manufacturing. The SRAM-based FPGAs are best suited for remote missions because of their reprogrammability by end users as many times as necessary in a very short time.

Cluster-based FPGA architecture can be used to model large design. In this work, we proposed a technique for detecting stuck-at and bridging faults in the Cluster-based FPGA architecture. Built-in-self-test (BIST) technique is a good choice to detect faults in FPGA based circuits. Researchers have divided the FPGA test problem into categories: *interconnect test problem* [11], and the *FPGA logic test problem*. The limited number of I/O pads greatly reduces test access from off-chip. This problem in the FPGA based architecture can be

Genetic Algorithm based Test Scheduling for Network-on-Chip*

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Abstract

Network-on-Chip (NoC) has emerged as a new paradigm for designing core based System-on-Chip (SoC). It supports high degree of reusability, scalability and has parallelism in communication. Reuse of the on-chip communication network is critical to reduce test cost. In this paper we present a Genetic Algorithm based approach to solve the problem of test scheduling for NoC. This method is based on the use of a dedicated routing path for the test of each core when an available on-chip network is reused as test access mechanism. Experimental results with the ITC'02 benchmark circuits show that GA produces schedules with lesser test times compared to other heuristics proposed in the literature.

1. Introduction

System-on-Chip (SoC) designed at nano-scale will soon contain billions of transistors. Consequently, the traditional bus based and point-to-point communication architectures become less attractive for systems where large number of pre-designed IP cores need to be assembled together into chips with complex functionality [1, 2]. In contrast to these methods, the Network-on-Chip (NoC) architectures consist of heterogeneous cores connected through an interconnection network [3, 4, 5]. It supports high degree of reusability, scalability and has parallelism in communication. The idea of accessing and reusing these resources during test was proposed in [6] and the results presented in that work show that much reduced test times can be achieved, while other cost factors such as pin count and area overhead are strongly minimized. The main advantage of the on-chip network reuse is the availability of several accesses to each core, depending on the number of system input and output ports used during test. Therefore, the reduction in the system test time is deeply related to the test parallelization. Despite the reduced test time achieved by the NoC reuse, improving the existing test scheduling approach to completely exploit the network parallelism has become a challenge. In this paper, we present a new test scheduling method using Genetic Algorithm.

The paper is organized as follows. Section 2 reviews some related works. Section 3 briefly explains basic concepts and notations of NoC. In Section 4, the Genetic Algorithm we use, its problem formulation and the cost function used for calculating the test time are briefed. Results follow in Section 5. Finally some concluding remarks for the work are reported.

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CV-based Analytical Modeling of Dynamic Power for 65 nm CMOS Library Characterization

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Abstract

Process variability and its impact on circuit design are of critical importance to address power management and optimization challenges for low power CMOS designs. The growing incidence of parameter variability in sub-100 nm CMOS designs has highlighted the need to consider the impact of dynamic power variations during design phase itself and hence to evolve variability-aware design methodologies. In this direction, we present an accurate and computationally efficient CV-model, based on capacitance-voltage (CV) characterization of MOS transistor, to estimate the dynamic power of a NAND gate. This model can then be used for characterizing the standard cell libraries for dynamic power. The CV-model is demonstrated for its adequacy and accuracy and it is shown that the model predicted dynamic power is in error by less than 4%, with respect to mixed-mode simulated results. The proposed CV-model is very useful in generating robust dynamic power distributions at the circuit level, for power budget sign-off, in nano-scale CMOS technologies.

Keywords: Process variations, dynamic power estimation, CV- based analytical modeling, CV-model, library characterization.

1. Introduction

Process variability and its impact on circuit design are of critical importance to address power management and optimization challenges for low power sub-100 nm CMOS designs. An explosion in gate count resulting due to increasing complexity and added functions, coupled with increasing performance requirements, have caused dynamic power consumption to multiply. From scaling theory, though active capacitance density is expected to increase by 43% per technology generation, in reality, it is increasing in the range of 30-35% due to less than 2X improvement in transistor density. As die size is also growing by about 25% per technology generation, the dynamic power is very significant and continues to increase (V. De and S. Borkar 1999).

Though the static leakage power dissipation is increasing with scaling and contributes about 33% of the total power consumption in sub-100nm high performance CMOS designs (G. Sery, S. Borkar and V. De 2002), dynamic power dissipation is still very significant and needs to be addressed in the presence of process variations. Several methods have been reported in the

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A Novel Efficient Power Optimization Method for Off-Chip Memory Access using Differential Memory Addressing

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Abstract

The power consumption reduction plays a pivotal role in embedded system's design, especially in case of portable mobile electronic equipments, where the demand for running more complex power voracious real-time applications are increasing with reduced device size and weight. To achieve this goal, the design of the system should be such that the power consumption is reduced or at least optimized at every stage of the system design. It is well known that in case of an embedded system, there is a significant amount of energy loss and delay associated with off-chip memory access. Many techniques have been developed in the past to address these concerns. In this paper, a new potential technique is proposed to reduce the power consumption, as well as the delay due to off-chip memory access. In the proposed method, priority has been given for sending of maximum numbers of Zeros (low state) via the address line for accessing the memory, which reduces the state transitions on each bus line.

1. Introduction

Today, because of great demand to run more and more complex power voracious applications on a portable battery driven system, the power consumption reduction plays a pivotal role in embedded system's design. Power consumed by any system without any useful result is considered to be wastage of power. The power consumption reduction provides several benefits like- it reduces generated heat, which reduces the problems associated with the increase

Leakage Modelling Of Logic Gates Considering The Effect Of Input Vectors

Janakiraman V[1], Bishnu Prasad Das[1], Vish Vishvanathan[2], Bharadwaj Amrutur[1]

Abstract

In this paper we present an accurate model for the leakage current of a logic gate using Neural Networks. Our model captures the effect of process variations, which include inter die and intra gate variations and the effect of supply voltage and hence it provides a very efficient tool for analysis of circuits that implement Dynamic Voltage Scaling (DVS). Further, for a particular gate, importance of leakage dependence on the input vector is brought out. We then present a technique to logically reduce the number of models by modelling different kinds of stacks present in the library. Results show that the neural network can model the distribution of the leakage current of gates to a high degree of accuracy with the error in mean being less than 1% and variance being less than 4%. It was found that Monte Carlo on our model was up to 150 × faster than Monte Carlo with SPICE.

Keywords: *Neural*, *Leakage, Modelling, Statistical, Sigmoid*

1. Introduction

Statistical analysis has taken over static analysis in digital design in nano-scale circuits, owing to the increasing impact of manufacturing variations. Statistical timing analysis has been studied in great depth for a considerable amount of time [10], but only recently has statistical leakage analysis gained some attention. As predicted in [1] leakage power will be a major contributor to the total power and shrinking transistor sizes makes this leakage power more difficult to predict. Variations in effective gate length, L_e, oxide thickness, T_{ox}, and threshold voltage V_{TH} can result in up to 20× variations in the leakage of the manufactured chips [2].

In the past few years considerable amount of work has been done in building models that predict leakage accurately. The empirical technique described in [3] captures the effect of variations in the effective gate length L_e and provides a simple analytical method to statistically analyze leakage but cannot handle variations in multiple parameters. [4] provides a generic framework to handle variations in multiple process/ random parameters but does not include deterministic variations like supply voltage. With extensive usage of Dynamic Voltage Scaling (DVS), a model that can capture variations for a range of voltages is very useful.

Another area of interest in the past few years has been the dependency of leakage current of a particular gate on the input vector combination. The most

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Dual Encoded Gray Coding Scheme and its application to non integral power of 2 depth Asynchronous FIFO

Salil Gadgil [1], Senthilkannan Chandrasekaran [2]

Abstract

Gray Codes are modified version of binary codes, which have the unique property of a bit change per count change. This is one of the important reasons why gray codes are used in handover over of signals from one clock domain to another in multi clock domain designs. This is done to avoid issues like loss of correlation, which are present inherently in synchronization of binary codes. However systems which implement gray code counters of modulo N, where N is not an integral power of 2, have the issues of correlation present. There are techniques like scalable gray codes that currently solve these issues however with limitations. We present an innovative method called "Dual Encoded Gray Coding scheme" which is largely scalable and overcomes limitations faced by the scalable gray coding mechanisms. We also demonstrate the application of "Dual Encoded Gray Coding Scheme" in an asynchronous FIFO where gray codes are largely used and compare it with scalable gray code scheme.

Keywords: Asynchronous FIFO, Gray Codes, Synchronization

1. Introduction

Gray codes have a distinct advantage in terms of only 1 bit change per count change. This becomes even more desirable when there is a need of synchronizing signals between multiple clock domains [1]. However, this is true when the mod N gray code counters have a value with N as an integral power of 2. When N is not an integral power of 2, there arises a need to have some additional techniques to reduce the risk of loss of correlation. Discussed in this paper are issues related to loss of correlation in binary counters and how the gray code counters solve the issue. Later we explain issues related to a modulo N gray code counter with N not an integral power of 2. We explain the existing technique for solving the above problem with its limitations. Finally we present the concept of the "Dual encoded gray code" and its application to asynchronous FIFO designs with its advantages and limitations.

2. Synchronization and Loss of Correlation

Synchronization is needed when a signal needs to be transferred from one clock domain to another. This is done to avoid meta-stability [2], [3] .Two-flop synchronizer is the most common and widely used synchronizer. In case of

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Incremental Connectivity Extraction for Large VLSI Layouts

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Abstract

In traditional CAD, a design needs to be recompiled from scratch after every update. Time to recompiling the design is proportional to the new size of layout and, not to the size of update. Generally these updates are local and affect only small parts of layout, so recompiling the whole layout may unnecessarily take lot of time. To reduce the design cycle time incremental algorithms are necessary. Incremental CAD algorithms search for the parts of the layout which are affected by the update and based on the previous results give the result of updates. But if the size of layout is so large that it cannot fit entirely into available main memory, the main performance bottleneck is the communication between fast internal memory and the slow external memory. There is need of algorithms and data structures which can use external memory management to reduce the external memory access and hence communication, between main memory and the external memory in terms of I/Os. In this paper, an I/O efficient and ***output sensitive*** *external memory algorithm for incremental connectivity extraction is presented. The main component of this algorithm is the proposed* ***recursive tiling*** *approach which provides an easy to implement data structure for the aggregation of parts of layout for fast search and updates.*

Keywords: External Memory Algorithms, Incremental Algorithms, Connectivity Extraction, VLSI Layouts

1. Introduction

In traditional CAD, the designers had to compile the design from scratch each time, after doing modifications. Time taken to recompile the design is proportional to the new size of layout. If the size of layout is large, recompiling the whole layout from scratch may take hours of CPU time. Incremental changes may be done on the design to improve the functionality of design or error correction, Coudert et al. (2000) and Cong et al. (2000). Generally these changes are local and affect only a small portion of the layout and its neighboring portions. So there is need for algorithms which will be able to compile the new modifications and give the results considering the previously compiled result, in short amount of time.

Traditionally algorithms and data structures are designed assuming that there is a large amount of memory available which requires constant time per access to any memory location. But this assumption may not be true in practice. The memory hierarchy of a computer system can be divided into a number of levels such as CPU registers, several levels of cache, RAM (main memory) and hard disk (external or secondary memory). These days there are many applications, including those of VLSI layout editing, which requires such a large

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Latency Optimized AES-Rijndael with Flexible Mode of Operation

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Abstract

The paper presents an efficient architecture of the Advanced Encryption Standard (AES-Rijndael) cryptosystem. The suggested architecture is capable of handling all possible combinations of standard bit lengths (128,192,256) of data and key. The proposed scheme employs a fully rolled architecture which has lesser hardware complexity compared to the existing ones. The design has been implemented on Xilinx Spartan III XC3S5000 as well as CMOS ASIC (front end) using 0.18µ COMS standard library. The experimental results show that the design performs favourably with the related existing work.

Keywords: AES, Rijndael, S-box, Composite fields, FPGA, ASIC

1 Introduction

The Rijndael block cipher [3] (capable of handling 128,192,256 bit blocks) was chosen as the Advanced Encryption Standard (AES) by the National Institute for Standard and Technology (NIST) in 2000. The AES algorithm (designed by John Daemen and Vincent Rijmen) is based on the symmetric block cipher. Compared to their slow software [2] counterpart, hardware implementation of AES-Rijndael is attractive, but it is costly.

Over the recent years many FPGA [4, 10, 12, 16, 17, 18, 21] and ASIC [4 - 7, 13, 14, 19] implementations for Rijndael has been reported. Most of them have used look-up tables to implement S-Boxes. Moreover almost all of them are unable to over the reconfigurability feature. The advent of composite field GF($(2^4)^2$) arithmetic in S-box operation was first noted in the works of Rijmen [3] and Rudra et al. [6]. Among the designers who tried to produce an area optimized implementation using composite field arithmetic, the work of Satoh at el. [7], Wolkerstorfer et al. [9], and Mentens et al [8] are of importance. Rudra et al. [6] implemented pipelined Rijndael over composite field GF($(2^4)^2$). Rijndael implemented by Rudra et al. supports only ECB mode of operation with 128-bit data. Debdeep at el. [5] has implemented 128-bit pipeline Rijndael over composite field GF($(2^4)^2$). But, it works on ECB mode of operation only. Satoh at el. [7] implemented AES-Rijndael which supports 128-bit data with ECB

On the Realizability of Specifications having Auxiliary State Machines and GR (1) LTL

Ansuman Banerjee, Pallab Dasgupta, P.P.Chakrabarti[1]

Abstract

In [8], Peterman et al. have identified a fragment of Linear Temporal Logic (LTL), known as Generalized Reactivity (1) (GR (1)), for which the realizability problem can be solved in EXPTIME. In this paper, we attempt to extend the GR (1) paradigm with the use of auxiliary state machines as part of the formal specification. This extends the expressibility of GR (1) LTL beyond simple Streett requirements, and makes it more practical and useful. The more interesting result, as we show here, is the fact that formal specifications consisting of auxiliary state machines and GR (1) LTL properties are contained in the GR (1) subset of LTL. We use the PCI and the ARM AMBA AHB protocols as case studies, and present results for realizability checking of these specifications, designed using the proposed modeling style.

Keywords: Realizability, GR (1) LTL

1. Introduction

The problem of checking realizability of Linear Temporal Logic (LTL) [9] specifications has been one of the most challenging problems before the validation community for decades and has been an area of active research. The high complexity of the LTL realizability problem, as established in the work [10] caused the problem to be doomed as highly intractable. In spite of the rich theory developed for realizability [1, 6, 10, 11], little has been reduced to practice. Yet there exist several interesting cases where, if the specification is restricted to simpler automata or partial fragments of LTL, it has been shown that the realizability problem can be solved in lower complexity. In [8], Peterman et al. have identified a fragment of LTL, known as Generalized Reactivity (1) (GR (1)), for which the realizability problem can be solved in EXPTIME. This is a significant improvement over the 2-EXPTIME complexity of realizability of LTL. However, this limits the expressive power of LTL to simple Streett [8] requirements.

In this paper, we attempt to extend the GR (1) paradigm with auxiliary state machines as part of the formal specification. The use of auxiliary state machines for modeling large and complex protocol specifications has been a popular practice [5, 13, 14] in the verification community in recent times, as observed by us from a study of the assertion IPs of a multitude of protocols (including ARM AMBA, Hyper Transport, IBM CoreConnect). Typically, a significant fraction of the correctness requirements in these specifications are only relevant in particular contexts of the protocol. Specifying such requirements entirely in terms of protocol signal values is not always easy. To circumvent this problem,

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Debugging Assume-Guarantee Specification for Compositional Verification

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Abstract

Though the design's architectural intent can be expressed in formal properties, those cannot be formally verified due to capacity limitations of formal verification. In an integrated verification flow, a set of lower level component properties are developed and are formally verified against respective component modules inisolation, modeling the environment as assumptions. As a result, a formal specification consisting of assumptions and guarantees of components, assumptions and guarantees of the entire design is developed. Finally, dynamic assertion based verification is performed on the integrated design. Often a number of properties, including those which were guaranteed at component level under certain assumptions, gets refuted during the later phase. In this paper we present: (1) a method for checking whether the specification is debuggable, that is, whether any failure of a formally verified property or of an architectural property can be attributed to violation of system level assumption by the testbench, (2) an approach based on counterexample-guided assumption refinement technique to identify the properties that need to be added to make the specification debuggable, (3) a method for identifying the root cause of failures of a set of properties.

Keywords: specification debuggability, root cause analysis, assume-guarantee

1. Introduction

Formal Property Verification [Clarke, Grumberg and Peled (2000)] allows the designer to express the key correctness requirements of a design in terms of formal properties and automatically verify them exhaustively over a given implementation. Unfortunately, FPV technology is poised at a peculiar position. The state explosion problem has restricted its usage within unit level design modules. On the other hand, anticipating all possible corner cases and discovering deeply buried design bugs have been one of the key verification challenges in simulation-based verification.

As none of the verification techniques can alone fulfill the goals, the current understanding is that the future of design validation lies in the symbiotic co-existence of formal and simulation based technologies. The first step towards FPV approach is to understand the design specification. The outcome of this step is the formal specification that contains a set of correctness requirements. The design's architectural requirements can be expressed in formal properties, however, due to the capacity limitations of formal verification, these architectural properties cannot be directly verified on the RTL. We apply traditional FPV approaches to validate the design components of manageable

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Formal Verification of Pipelined Read-Modify-Write Logic by Generalized Symbolic Trajectory Evaluation (GSTE)

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Abstract

We report the verification of a complex pipelined data path design using GSTE model checking. We have enhanced an implementation of STE available as a public domain tool, FORTE, to support GSTE. We report key implementation details. The data path design which has been verified is a 4 stage pipelined Read-Modify-Write logic. Complex properties which are spread over infinite time intervals are specified and verified. The verification time is improved by carefully reducing the number of precise nodes used to perform reachability analysis, while providing complete state information to the symbolic simulator. We report performance results, in terms of the memory usage and CPU time, for key components of the verification tool. These results prove viability of the GSTE methodology as a formal verification technique for control dominated designs such as large scale pipelined data paths.

Keywords: *GSTE, parametric representation, precise nodes, symbolic constants, symbolic variables, assertion graph.*

1. Introduction:

Formal verification techniques such as, symbolic model checking and theorem proving have met with limited success because of intrinsic problems related to state explosion and the need for manual intervention, respectively. Even though STE is less sensitive to state explosion problem and proven to be a viable methodology for large scale data path verification, it suffers from the problem of inexpressibility. Properties which are spread over infinite time intervals cannot be expressed in STE, let alone be verified [1-3]. GSTE constitutes a very significant extension to STE. It has been used successfully by INTEL on its new generation microprocessor designs. GSTE addresses the drawbacks of STE and has the power to verify complex assertion graphs with which any ω-regular property can be equivalently represented, while at the same time it preserves the benefits of STE, like the insensitivity to state explosion, thereby capturing the expressiveness of classical model checking [4-6] and [8]. This paper focuses on the internal details of our implementation of GSTE and its application to a pipelined design. To the best of our knowledge, this is the first time that the GSTE methodology has been applied in the verification of a pipelined data path design. The paper is organized as follows. Section 2 presents the implementation details of the GSTE methodology. Section 3 elucidates the motivation to choose the Read-Modify-Write logic as a case study and gives the functional overview of the design. Section 4 describes the designs formal specification in terms of assertion graphs. In Section 5, we present results establishing GSTE's viability as a potential formal method for verifying control dominated designs such as,

An Efficient Implementation of Testbench for Verification of Configurable Host Controller IP addressing Mobile Storage Applications

Pusuluri Giri Kumar

Abstract

The functional verification of configurable host controller IP, such as host controller supporting multiple protocols (SD/MMC/CEATA), is a challenging task. The challenge lies in identifying the hidden bugs in verification phase. Some of the bugs are deeply embedded and can be detected only with a sequence of transactions like error transaction followed by normal transaction. Traditionally verification engineers develop the discrete error tests to cover the error scenarios and are run separately. This approach tends to fail in detecting the sequence dependant bugs. The detection of sequence dependent bugs is a two dimensional problem in verification. Firstly the testbench may not be capable of generating a mix of normal and error transactions. Secondly the testbench driver may not be capable of injecting the errors and also automatically recover from the error state to normal state to support the stream of random transactions which includes normal and error transactions.

In this paper, the author proposes a practical solution to the above mentioned verification problem. The focus of the solution lies with the design and implementation of the transaction generation model and the testbench driver. The transaction model discussed in this paper is capable of generating a stream of random transactions which is a mix of normal and error transactions. The error recovery mechanism is defined and implemented in the testbench driver which has shown definite improvement in the quality of verification. The testbench is implemented based on the Reusable Verification Methodology (RVM) guidelines.

The proposed transaction and driver models are implemented and used to verify our configurable host controller IP for mobile storage applications. We were able to successfully detect the hidden bugs in the verification phase.

1. Introduction

The emerging mobile storage technologies enable high capacity storage devices (compliant to protocols like SD [1], MMC [2] and CEATA [3]) to be integrated into the devices like digital cameras, MP3 players. The physical interface for these memory devices remains the same but the communication protocol varies; hence the host controllers should be configurable to be interfaced with mobile storage devices.

Scenario Driven Test Case Generation for Functional Verification of Pipelined Processors

S. K. Panda[1], Venu Gopal Kasturi[1], P. P. Chakrabarti[1] and Rajeev Kumar[1]

Abstract

In this paper, we present a novel approach to generate test cases for functional verification of pipelined processors; which drive the pipeline into scenarios described by the user in a high level language defined using predicates. The predicates are instantiated to obtain a state of the pipeline which represents the scenario specified. An algorithm has been proposed to generate hazard free test programs i.e. programs which drive the pipeline into the desired scenario without stalling it in the path of reaching the scenario. A frame work has been developed and test programs are generated for the VLIW-DLX architecture.

Keywords: Verification, Pipelines, Test-Generation

1. Introduction

The complexity of verification of pipeline processors is growing in leaps and bounds due to the technological advances in optimizations and algorithms developed to introduce parallelism at the instruction level. This also increases the need for rigorous testing of the processor design. Verification of the processor at the functional level is quite important because it then obviates a majority of design level errors. Designers would want to test the processor for critical conditions where instructions interact with each other i.e. cases where there can be hazards, exceptions etc. and there would be situations where they want to test a specific type of scenario extensively.

For verification of the pipeline, random test pattern generation could prove to be costly because coverage is not guaranteed. A large number of test cases are needed which could lead to a huge number of cycles spent in testing. Few approaches involve using the finite state machine of the pipeline and generating test programs for a subset of the reachable states. In [1], a Finite State Machine (FSM) model of the pipeline is used. The stall conditions are mentioned explicitly and image computation techniques are used to generate test programs for every reachable state of the pipeline. But we need not generate test programs for cases which are not critical to the logic of the pipeline. In [2], the functional units are modeled as states of an FSM. The state of a unit is denoted by the instruction it is executing. And then the test programs are generated by the image computation technique. In [3], Mishra et. al, generate functional test programs based on the coverage of the pipeline behavior. Test generation time is drastically reduced due to the use of module level property checking. In [4], a

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Leakage and Switching Power Minimization with Area Trade-off in Multiplexer Based Circuit Synthesis

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Abstract

Due to regularity of implementation, multiplexers are widely used in VLSI circuit synthesis. This paper proposes a technique for decomposing a function into 2-to-1 multiplexers performing area-power tradeoff. To the best of our knowledge this is the first ever effort to incorporate leakage into power calculation for mux-based decomposition. With respect to an initial BDD based representation of the function, the scheme shows about 50% reduction in area, leakage and switching for the LGSynth91 benchmarks. It also enumerates the trade-offs present in the solution space for different weights associated with these three quantities.

1. Introduction

Multiplexers have long drawn the attention of VLSI design and research community to realize the final circuit. This is mainly due to the high regularity of multiplexers that make the structure particularly suitable for VLSI implementation. Introduction of low-power regime has brought with it further challenges due to the increased usage of portable, handheld, battery-operated, plastic-packaged devices. This type of devices necessitates low-power consumption for increased battery life, low-cost and so on. Due to this, researchers have been motivated to look into the multiplexer decomposition problems [3, 4, 5, 6]. In these works, a large multiplexer is decomposed into a tree of 2-to-1 muxes. While [5] and [6] dealt with delay minimization, [3] handled the problem of power-efficient decomposition. However, none of these handled multi-output function-which is the most common structure in any digital system. [12] proposed a methodology to synthesize multi-output function using 2-1 multiplexers. The work also performed a trade-off between the area of the resulting circuit (in terms of number of 2-1 muxes) and the dynamic power consumed (measured as estimated switching activity over all multiplexers). However, the work ignored the leakage power consumed by the circuit under the premises that leakage power is quite insignificant as compared to the dynamic power. The International Technology Roadmap for Semiconductors (ITRS) projects an exponential increase in the leakage power with minimization of devices [2]. As the technology drops below 65 nm feature sizes, subthreshold leakage is expected to exceed the total dynamic power. As leakage current becomes the major contributor to power consumption, the industry must reconsider the power equation that limits system performances, chip sizes and cost.

In this paper we have presented a multiplexer targeted circuit synthesis scheme that thrives to attain the minimization of both dynamic and leakage power. To

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A NOVEL TOGGLE LESS, LUT-LESS LOW POWER DISTRIBUTED ARITHMETIC (DA) ARCHITECTURE FOR FIR FILTER

Uma Rajaram[1], P. Augusta Sophy[2]

ABSTRACT

This paper proposes a new DA (Distributed Arithmetic) architecture for FIR filter which exhibits both area and power efficiency. Many DAA (Distributed Arithmetic Algorithm) based architectures have been proposed for building an FIR filter so for. The performance of the various DA architectures has been studied and a new DA architecture with maximum area and power efficiency is proposed. The suitability of the FPGA architecture for DA is found in terms of area utilization and power consumption. Conventional FIR filter, Serial DA, Two-LUT DA (50% ROM size saving), and LUT-less DA are implemented to study the area efficiency. Serial DA, 'Non-uniform memory' DA, 'Shift-less registers method' and a 'NewDA for Low power' is implemented and their performance is analyzed. A novel architecture with shiftless registers and LUT-less technique has been developed and implemented. This architecture shows 100% ROM area saving, up to 88% less gate count and a maximum power saving of 29%.

1. INTRODUCTION

High-speed digital filtering applications generally require dedicated hard-wired implementation of the filters. Programmable processors can provide high sample rates only with excessive amount of parallelism, which may not be cost effective. Recently hardware implementations of DSP algorithms on FPGAs are gaining increasing popularity since they provide both a programmable and a dedicated hardware solution.

A discrete-time linear finite impulse response (FIR) filter generates the output Y[n] as a sum of delayed and scaled input samples X[n]

$$y[n] = \sum_{k=0}^{N-1} A_k X[n-k] \qquad (1)$$

This formula actually describes only a single output at instance nT in the infinite time. A_k is the kth coefficient of the polynomial and represents the system impulse response, and x_k is the kth input sample at time n. Each output is equal to the sum of k products. A direct VLSI implementation requires N multiply and accumulate (MAC) operations, which are expensive to implement in hardware due to logic complexity and area usage. Alternately the MAC operations may be replaced by a series of look-up-table (LUT) accesses and summations, known as **distributed arithmetic (DA).** DA is a bit serial

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A Core Power Pad Planner for Wirebond SoCs

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Abstract

A core power pad planning approach is presented for system on chips with wirebond packages. The approach can be used very early in design cycle viz] during the floorplan prototyping stage. The number of power pads and their distribution over the chip periphery is optimized by iterating over, the DC analysis of the power grid for a worst case static IR drop. The current in these pads are also bounded by Electron-Migration (EM) limits. The proposed approach can handle different types of constraints, including those arising from periphery, floorplan and power domains. The approach can also be used for various what_if analysis involving constraint debugging A methodology is presented for computing sensitivities of source locations to prove the robustness of the solution. Results have been shown for different design scenarios.

Keywords*: SoC, ASIC, Power Grid, IR Drop, SPICE*

1. Introduction

Power network design for SoCs has become a very challenging activity with shrinking feature sizes. Multiple power domains, power management, multiple package targets and stringent constraints on performance, force requirements for a robust power network design. In the case of wirebond SoCs, this constraint also becomes equally important from a source count and distribution standpoint. IO power pad requirements for a design is based on worst case switching of output buffers at the interface of the design. However for core power domains, it is based on IR drop requirements of the design. In this work we focus on estimating power pad count and distribution for core power domains.

Closure of IR drop in power grids for an SOC can be achieved by posing it as an optimization problem involving power pads and the power network. However lack of efficient source planning capabilities, force designers to over-design the power network to meet electron migration (EM) and IR drop requirements. This can be easily solved through better pad planning. As this change can result in a major cycle time impact, this vector of optimization is not looked upon as a viable option. This provides a strong motivation for our present work. To the best of our knowledge almost no similar work has been reported in this area excepting for [1], [2]. Similar work has been reported on source based grid optimization in [3], [4], [5] and [6]. Although source locations and current sinks are considered in these papers, however constraints to handle these scenarios have not been explored. We explain these constraints in a later section.

Design of an Application Specific Low-Power High Performance Carry Save 4-2 Compressor

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Abstract

This paper proposes a new 4-2 compressor for high speed and low-power multiplier application. This compressor circuit is totally different from the conventional 4-2 compressors. It is essentially a single bit adder having four inputs and three outputs and is built entirely around transmission gates. It is based on the observation that a single bit adder is nothing but the counter of 1's at the input bits. Conventional 4-2 compressor entails two full adder delays while our proposed compressor produces a delay that is slightly greater than that of a single FA but is much less than that of two full adders.

Simulation results show that the proposed 4-2 compressor is able to function at a supply voltage of as low as 1 volt. It is also much faster than CMOS 4-2 compressor and differential pass transistor logic (DPL) compressor. Above all it has the same and simple philosophy as that of 3-2 counter or a single bit (three-input) FA.

Keywords*: 4-2 Compressor, TG, DPL, Adder, Logical effort, DTCMOS.*

1. Introduction

Now-a-days many digital signal processing (DSP) systems are made portable, battery operated systems. Power optimization plays a key role in the design of such circuits. In many DSP applications, multiplication is the basic arithmetic operation, the primary requirement being speed. However, battery operated mobile microprocessor and DSP systems require fast as well as low power multipliers.

A multiplier can be divided into three stages: partial product generation stage, partial product addition stage, and the final addition stage. The second stage of the multiplication process requires adders or compressors and this stage mainly contribute to the delay and power. In this stage, the Wallace tree [1, 2] construction method is usually used to add the partial products. 4-2 compressors are used in this tree construction to reduce addition stages and hence to reduce the delay.

In this paper we propose a new compressor architecture in order to satisfy the requirements of low power and high speed for multiplier.

2. 4-2 Compressor architecture

The conventional 4-2 compressor structure actually compresses five partial product bits into three [2, 3, 4]. The architecture can be implemented with two

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A Transformation Based Method for Formal Analysis of Hybrid Systems

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Abstract

Formal verification of hybrid systems containing discrete and continuous time domain components, traditionally has been based on simulation, through discretization of time, to obtain the solution of differential equations characterizing such components. In this paper an alternate approach is proposed. This approach is based on linear transformations applied to certain classes of dynamic components which remove the time discretization step needed in simulation based solution of differential equations. This approach can be easily embedded in the analysis of hybrid systems modeled as timed or hybrid automata. State variables corresponding to dynamic components are assumed to be described by linear differential equations in space and time. Residue decomposition obtained through partial fractions of the algebraic expressions in the transformed domain is then used to solve these linear differential equations. The resulting exact solutions are then combined with the state variables corresponding to the discrete components to formally validate safety properties of hybrid systems. This methodology is illustrated by analyzing a hybrid system describing an adaptive cruise controller used in automobiles.

Keywords*: SoC, Microsystem, Hybrid Systems*

1. Introduction

Formal verification of hybrid systems has been an area of active research [1] [2] [3] [4]. Hybrid systems are characterized by continuous time differential equations which work concurrently with discrete time digital systems. Modeling of such hybrid system involves modeling both discrete, as well as, the continuous time, or dynamic behavior. Most approaches to modeling hybrid systems is based on extending finite automata used for modeling discrete behaviour to include simple continuous behaviour. Examples include timed automata [5], linear hybrid automata [6] and hybrid input/output automata. Validation of hybrid or embedded systems is carried on such models and primarily involves the stringent verification of the behaviour of safety-critical system components [2]. Safety verification is encoded as a constraint on the region of operation in the hybrid systems state space representing unsafe operations. Essentially, the hybrid system, under no condition should be able to reach this unsafe state space from any of its legal set of initial states. Thus, validation for safety critical behaviour implicitly involves determining the reachable set of states of the hybrid system, just as in the case of discrete time systems such as digital systems.

Determining the reachable set of states of a hybrid system constitutes one of the most important problems in its verification. While the computation of reachable

Embedded Tutorial : Formal Verification of DFT Logic and their Integration in System on Chips – Practices, Issues and Challenges

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Abstract

This embedded tutorial presents the methods and challenges for modeling DFT (both BIST and non-BIST) logic in complex SOCs to enable their verification using formal techniques. The main areas of focus in this tutorial is towards, (a) application of symbolic model checking to DFT IPs and DFT logic verification, (b) enabling property based formal verification through abstraction and modeling of generic sequential blocks such as memories, data-loggers, scan chains, LFSRs, and generic DFT logic sub-modules such as Test Interface, JTAG based TAP controllers (IEEE1149.1/IEEE1150) with interface and data registers, Pin Multiplexing together with other boundary scan and switch fabric logic, PLL controller and clock generation logic for various test modes, controllers for selection of multiple TAPs, (c) automated generation of re-usable properties for DFT logic and their hookup logic, where-ever applicable, and (d) case studies to highlight the benefits of the proposed techniques. These techniques have been applied to verify DFT logic and their integration in different SOCs designed in Texas Instruments India, with promising results.

Keywords*: SOCs, DFT Logic, DFT Integration, Formal Verification, Symbolic Model Checking*

1. Introduction

Present generation systems on chip (SOC) designs are built hierarchically with a large number of embedded memories of different kinds and sizes and different embedded cores (e.g. processors, peripherals, etc.) each having different content of I/Os, logic and memories. To reduce expensive ATE time, post manufacturing silicon testing of these blocks is often done using built-in self-test (BIST) techniques, namely, memory BIST and logic BIST, respectively [1-3, 7]. These are suitable for a variety of reasons, including for low pin count testing, embedded core test, etc. Test application using BIST controllers can often be lengthy (over several tens of thousands of cycles and states) depending upon the test sequences generated by the controller, resulting in large verification times for large controllers. The controller construction is itself largely independent of the circuit under test (CUT). This highlights the three main characteristics of controllers which are of interest, namely, (a) their large sequential depth, (b) their canonical structure, and (c) the generic nature of their hookup to the CUT. These underlying characteristics can be exploited, to enable the formal verification (FV) of DFT blocks consisting of BIST controllers and non-BIST logic having generic customizable, configurable and parametrizable structures, and their integration into SOC designs.

Commercial tools are used to automatically generate and integrate memory and logic BIST controllers into the design in RTL form or gate level net-list form. These tools use a scripting language based description of the embedded

HYBRID MASKED KARATSUBA MULTIPLIER FOR $GF(2^{233})$

Chester Rebeiro[1] and Debdeep Mukhopadhyay[2]

Abstract

The paper presents a detailed study on the implementation of Karatsuba Multiplier for GF (2^{233}), which is a state of the art field for secured Elliptic Curve Cryptography, according to NIST. The work suggests the trade-offs involved in designing this important class of multiplier and proposes a Hybrid Karatsuba Multiplier which requires least amount of space on a FPGA. The work also shows a novel masking technique to prevent the multiplier from power based side-channel attacks. Comparison shows that the proposed scheme requires lesser number of gates compared with the conventional approach.

Keywords: Karatsuba Multiplier, Elliptic Curve Cryptography, Masked Multiplication

1. Introduction

Elliptic Curve Cryptography (ECC) was invented independently by Koblitz and Miller in 1985. Since then, the security and efficiency of ECC has been proven, and ECC has been incorporated in several security standards. ECC offers more security per key bit than any other public key cryptosystem. This has prompted the U.S. National Security Agency to move to ECC based public key cryptography. For a given level of security, the size of the key and the operations involved in ECC computation is much shorter than other crypto algorithms. This makes ECC an attractive alternative for today's hand held devices where processing bandwidth, memory resources and power are limited.

NIST's standard for Digital Signatures [1] recommends using a prime field, $GF(p)$, or a binary extension field $GF(2^m)$ for Elliptic Curves. Binary Extension Fields have the advantage that field additions can be performed by *XOR* operations, therefore no carry is involved. This leads to implementations that require lesser area and have better performance. The NIST standard recommends binary extension curves of degree 163, 233, 283, 409 and 571. For our work on the implementation of Elliptic Curve Cryptosystem on a FPGA, we have selected the field $GF(2^{233})$ as there have been very few published works [3] for implementations specific to this field.

Implementation of Elliptic Curve Cryptosystems follows a layered hierarchical scheme as shown in Figure (1). The performance of the top layers of the hierarchy is greatly influenced by the performance of the underlying layers. It is therefore important to have efficient implementations of finite field operations such as additions, multiplications and inversion.

There are several methods to implement the finite field multiplication such

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PRIORITY QUEUE BASED LRU MODELS FOR ASSOCIATIVE CACHE

Vijayalakshmi Seshadri[1]

Abstract

With the implementation of LRU for associative cache becoming a bottleneck for performance, efficient structure is needed to maintain the LRU history and to easily access the line of replacement. Priority queue data structure favors the retrieval of element of high priority element in 0(1) time by placing the element in the root node and it is currently being deployed in many applications including packet scheduling algorithms in networks, discrete event simulations, process scheduling in operating systems. This paper uses this property of priority queue to model the implementation for LRU, making it best suited for associative cache. Priority queue property and operations are modified to support hardware implementation of LRU and three efficient priority queue based LRU models for associative cache -Sorted list, Pipelined Heap, Pipelined d-Heap are proposed, designed and implemented for various associativity with various cache size and are compared among themselves and with the existing and previous implementations. Sorted list is a good option for low associativity cache due to simpler implementation and memory needed to maintain the LRU history is less .It does not scale well as associativity increases and maximum clock frequency of 128.1Mhz is obtained for 8way associativity. Pipelined heap is a Pipelined d-heap model where d value is 2 and rearrangement of structure is done in both pipeline and parallel fashion. It scales well as associativity increases and gives performance of maximum clock frequency 109.1Mhz and number of gates around 10k for 256way associativity. The choice of the correct d – value for associativity increases performance.

Key Words: *High associativity, Heap, LRU, Priority Queue.*

I. Introduction

Caching is used to hide and tolerate the speed gap between processor and memory [1] and various schemes have been proposed to increase its performance and one among them is increasing associativity of cache [2,3,4]. Studies show that increasing the cache associativity reduces the miss rate, power consumption and thrashing [2,3,4,8] and are deployed in the systems where miss penalty is large and memory interconnect delay are significant [9]. But with associativity comes the question which replacement strategy to use [8]. Among the most common replacement policies LRU significantly reduces the misses, and approximates to optimal replacement policies [10]. But LRU is not algorithm of choice for all situations. For two-way associative cache the LRU history can be maintained in a single bit called access bit, where value one in the bit represents it is most recently used and zero representing it is least recently used. For four-way associative cache, LRU history can be maintained using

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A New Spice Simulator for Single Electron Transistor Based Integrated Circuits

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Abstract

Single Electron Transistor (SET) has attracted much attention as a strong candidate for post CMOS VLSI. Successful implementation of SET therefore demands accurate analytical modeling and efficient circuit simulation platform. This paper for the first time, reports a spice simulator for SET based integrated circuits which uses analytical SET models instead of Monte Carlo (MC) simulation .The existing SET simulators are based on MC and Master equation methods which are time consuming and have limited possibility for simulating complex hybrid CMOS-SET integrated circuits. The simulator is a C-based simulator which is much faster as it considers SET as a piecewise linear device and represents it by a variable resistor. The resistance value is determined from the well-established $I_D - V_{DS}$ characteristic given by analytical MIB model. The accuracy of the simulator is tested for several standard SET circuits (e.g. SET inverter, long chain inverters, Current biased SET, and negative differential resistance device (NDR)) and agrees with a high degree of accuracy with MC, and Verilog-A simulations.

Keywords: Single Electron Transistor, Monte Carlo, compact model

1. Introduction

Single Electron Transistor has appeared as an attractive candidate for extending the CMOS lifetime beyond the 10 nm brick wall as predicted by ITRS [1]. SET based circuits are gaining popularity due to extremely low power dissipation, unique Coulomb Blockade oscillation property and compatibility with existing CMOS process flow.

A schematic of a SET, which consists of a tiny conductive island, two highly resistive tunnel junctions, and an opaque gate is shown in Fig. 1. It is worth noting that the operation of the SET devices is based on the *Coulomb Blockade* phenomenon [2], which is quite unique compared to the principle of operation of MOS transistors. By exploiting this phenomenon, several *niche* applications of SET devices have been demonstrated in logic circuits, analog circuits and in mixed signal circuits regime [3].

CMOS and SET are quite complementary to each other, SET is a campaigner of low power dissipation [4,5] and novel functionality while CMOS has higher voltage gain and operation speed that compensates for the intrinsic drawbacks

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FABRICATION OF MEMS PZR ACCELEROMETER FOR AUTOMOBILE APPLICATION

R. Mukhiya[1], I. S. Bajpayee[1] and S. Kal[1]

Abstract

A bulk-micromachined piezoresistive accelerometer for single axis ±2g (out of chip plane) with low cross-axis mechanical and electrical sensitivity has been fabricated. The accelerometer structure is highly symmetric and consists of eight p-type embedded piezoresistors in <110> direction and electrically connected to minimize the cross-axis sensitivity to form Wheatstone bridge. Fabrication process derived and simplified from the standard CMOS process and extended for post-CMOS compatible bulk-micromachining. Non-conventional single step double sided micromachining is performed using dual-doped (SA + AP) 5% TMAHW solution at 90°C. The three layer glass/Si/glass bonded accelerometer has a size of 11.5 mm X 8.5 mm X 1.3 mm.

Keywords: MEMS,Accelerometer Fabrication,Bulk-micromachining.

1. Introduction

Miniaturized micromachined accelerometers are very attractive for space navigation, automobile applications and defence applications, because of its size, weight, batch fabrication and power advantages [Navid Yazdi et. Al. (1998), Davis S. et. Al. (1998)]. Among different approaches to realize accelerometers, two approaches are well-advanced and commercialized, viz.; one is piezoresistive type and another is capacitive type. Each of this two has its own advantages and disadvantages, but piezoresistive is much more attractive because of ease of fabrication and signal pick-up, though, it suffers from the cross axis sensitivity [H. Crazzolara et. Al. (1993), H. Seidel et. Al. (1990), K. Yamada et. Al. (1990)].

Most common structures of piezoresistive accelerometers are cantilever beam, quad beam and two-mass five beam structures [Hing Chen et. Al. (1997)]. All these structures are beam-mass structures with horizontal beams fabricated on (001) silicon wafer. Beams are flat in <110> direction and on the top surface of the wafer to place p-type piezoresistors. This technological limitation of placing beams above the plane of centre of gravity in piezoresistive accelerometers causes cross-axis sensitivity. In the present design quad beam symmetric structure is preferred to make the sensor mechanically less cross-axis sensitive and beams are positioned in such a way that results in higher modes, accept the first mode. In the reported quad beam accelerometer structures, the beams were placed inside the edges of proof mass because of less complexity in the wet bulk-micromachining [S. Kal et. Al. (2006)].

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BULK-MICROMACHINING FOR MEMS ACCELEROMETER USING 25% WT. TMAH

R. Mukhiya[1], M. Zen[2] and S. Kal[1]

Abstract

In the present work, experimental study to realize bulk-micromachined Si based MEMS accelerometer structure is presented. Technological problems associated with bulk-micromachining to fabricate such type of structures are presented and their solutions are proposed and verified experimentally. For study symmetric MEMS accelerometer structure is used, which has four flexures placed at the edges of the proof mass in <110> direction and truncated pyramidal proof mass (mesa type). Experiments were carried out using 25% wt. TMAH-water solution at 90±1^{0}C temperature. Convex corner undercutting, fast etch planes, etch rates of different crystal planes and corner compensation structures, their space requirements and imprint interaction with beam routes are presented. At flexures root locations compensation structures have most adverse effect on the structural performance and feasible solutions are experimentally verified.

Keywords: MEMS,Micro-sensors,Bulk-micromachining,Accelerometer,Corner Compensation (CC).

1. Introduction

Bulk-micromachining is a great concern to the researchers and industries to fabricate silicon micro-sensors from a long time. Among different bulk-micromachining techniques chemical wet etching is the most popular, because it is simple and cost effective. Most of the reported work is concentrated on KOH anisotropic etching and recently interest is growing towards TMAH anisotropic etching, because of its CMOS compatibility and on chip integration with electronics is possible [Tabata O, Asahi R, Funabashi H, Shimaoka K and Sugiyama S (1992)].

In wet chemical etching compensation structures leave undesired imprint and masses and require some study; especially in the case where structures are to be integrated with thin membrane and beams. How these imprint and their effect varies with compensation structures are not reported very well. Little investigations have been made on corner compensation for TMAH anisotropic etching and their imprint interaction with beams root. Present work has been carried out to study the related issues for bulk-micromachining of silicon for 25% wt. TMAH.

In the reported work mesa type of structures with beams were realized by using two step conventional chemical etching. First from back side etching

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Design, Modeling and Simulation of High Performance RF MEMS Switch for Phase Shifter Applications

Avra Kundu, Swati Majumder, Bhaskar Gupta and Hiranmay Saha*

Abstract

RF MEMS shunt capacitive switches have strong potential for application in Phase-Shifters for radar and many other communication systems because of its superior characteristics as compared to conventional semiconductor devices. However, they suffer from unacceptably high actuation voltage and relatively slow switching speed. In this paper we report the design and simulation of two novel structures of RF MEMS capacitive shunt switches namely Fin and Spring structures whose actuation voltage are significantly lower (18V and 8V respectively). The RF performance such as insertion loss, return loss and isolation have been analyzed in detail and found to be excellent. The isolation in particular for the Spring structure is extremely high because of its inductive like meander. The entire simulation has been carried out in ANSYS and IMST EMPIRE XCcel.

***Keywords**:* RF MEMS, Capacitive shunt switch, low k- structures, Inductive tuning.

1. Introduction

MEMS are now being increasingly used in modern radar and communication systems for their superior performances as low loss RF switching devices and variable capacitors compare to the GaAs, MESFETs and PIN Diode counterparts [1, 2]. MEMS switches enjoy several advantages over semiconductor switches in the RF applications namely (a) contact and spreading resistances are eliminated resulting into low resistive loss, I-V non linearity is absent leading to reduction in distortion characteristics and improved power handling capacity and negligible quiescent current consumption [3]. However, MEMS switches suffer from a number of limitation: (a) high actuation voltage of about 30-120 V which is too high for other CMOS circuits (b) low switching speed of about few microseconds.

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CHARACTERIZATION OF UNIVERSAL NAND-NOR INVERTER

Bibhash Sen[1] and Biplab K Sikdar[2]

Abstract

This paper introduces a QCA structure realizing a universal gate. The proposed 3-input QCA gate is referred to as the Nand-Nor-Inverter gate NNI(A,B,C)=maj(A',B,C')=A'B+BC'+C'A'. The functional completeness of NNI is demonstrated with the realization of logical NAND, NOR and Inverter functions (the fundamental logic gates). The characterization of NNI is carried out to focus on the reward of using such gate in designing the logic circuit than that of conventional AOI (And-Or-Inverter) QCA structure.

Keywords: Quantum-dot cellular automata, nand-nor-inverter gate, majority gate, AOI, QCA tile.

1. Introduction

The CMOS technology will reach to its fundamental limit in dimension [1]. The researchers are looking for a radically new technology. Quantum-dot Cellular Automata (QCA) [2], [3], [4], [5] appear to be the promising technology for future generation ICs. Such a technology is expected to achieve a density of 1012 devices/cm^2 with operating speed at the order of THz.

A number of approaches, targeting design & synthesis of QCA based logic circuits, has been reported in [3], [5], [6], [7], [8]. The fundamental unit of such designs is the 3-input majority gate (majority voter). However, the 3-input majority gate MV =maj(A,B,C) =AB+BC+CA is not a universal gate. It can not realize the logical NOT operation. The designers have to consider a separate costly QCA cell arrangements for realization of the logical NOT.

In [9], Momenzadeh et. al. have reported a configuration with 7 carefully arranged cells to realize the 5-input AOI (And-Or-Inverter) logic. Functionally, it is a combination of two majority gates and one of these majority gates works on complemented inputs. The careful arrangement of cells in AOI demands proper separation of input/output wires so that these do not interfere with each

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A LIFTING BASED RECONFIGURABLE FORWARD AND INVERSE DISCRETE WAVELET TRANSFORM ARCHITECTURE FOR JPEG2000

Yogesh Inamdar, Ramesh Kini. M.

ABSTRACT

The image compression standard JPEG 2000, has adopted DWT as its transform coder. JPEG2000 uses two lifting based wavelet transform kernels as its transform coders. These are the lossless 5/3 filter and the lossy 9/7 filter. In this paper, a reconfigurable architecture for computing the 1-D forward and the inverse transforms for both 5/3 and 9/7 wavelet filters has been proposed. The architecture is a folded reconfigurable one and combines both the 5/3 and 9/7 filter structures into a single hardware entity. The 1-D core is extended to 2-D by using simple row-column architecture. The 2-D architecture has been implemented on TSMC 0.13µm 8 metal layer technology.

1. INTRODUCTION

Wavelet analysis is being used in wide range of multimedia applications like signal analysis, audio signal processing, and image compression. Significantly, the two dimensional (2-D) biorthogonal Discrete Wavelet Transform (DWT) has been adopted in the JPEG2000 still image compression standard. Since the DWT is implemented using filter bank, it requires extensive operations. To reduce these operations, a new scheme called lifting scheme was proposed [1].

To provide an efficient lossy and lossless compression within a single coding architecture, two wavelet transform kernels are recommended in Part-One of the JPEG2000 standard. These are the lossless 5/3 filter and the lossy 9/7 filter. The implementation is based on the lifting scheme. There has been a tremendous amount of interest in developing 1-D/2-D lifting based architectures for these filters. However, most of these architectures target the implementation of one particular type of wavelet filter, i.e. either the 5/3 or the 9/7. Clearly, it is feasible to implement them on a unified architecture. This is achieved by what is called a folded reconfigurable architecture [2].

It has been observed that very few architecture exist that compute both the forward and inverse transform for both 5/3 and 9/7 wavelet filters on a single core. [3], [4] suggest a unified forward and inverse architecture for only the 9/7 transform. [5] suggests separate architectures for forward and inverse transform. The JPEG2000 decoder uses IDWT for image decompression.

MoTSoC: Mesh-of-Tree based Network on Chip Design
A New Interconnection Structure for SoCs*

S. Kundu[1], M. Sathi[2] and S. Chattopadhyay[3]

Abstract

Network-on-Chip (NoC) architectures consist of heterogeneous cores connected through an interconnection network. The communication between the nodes is achieved by routing packets rather than wires. It supports high degree of reusability, scalability, and parallelism in communication. In this paper, we present MoTSoC, a scalable NoC architecture based on Mesh-of-Tree (MoT) deterministic routing. Mesh-of-Tree interconnection network has the advantage of having small diameter as well as large bisection width. It is known as the fastest network when considered solely in terms of speed. The routing algorithm ensures that the packet will always reach destination through the shortest path. To the best of our knowledge, this is the first ever effort to build a MoT interconnection structure for NoC design.

1. Introduction

System-on-Chip (SoC) designed at nano-scale will soon contain billions of transistors. Consequently, the traditional bus-based and point-to-point communication architectures become less attractive for systems where large number of pre-designed Intellectual Property (IP) cores need to be assembled together into chips with complex functionality. Since on-chip communication architectures have a significant impact on system performance, designers have focused on SoC communication architectures to meet the targeted design goals. One emerging solution is the integrated switching networks, called Network-on-Chip (NoC), to interconnect cores in SoCs. The communication templates typically used in current SoCs are bus-based. However, a bus does not scale with the system size and its bandwidth is shared by all the systems attached to it. Secondly its operating frequency degrades with the increasing number of cores attached. Thirdly, the power consumption increases with the circuit size. Finally a bus allows only one communication at a time, and even in a hierarchical bus, a single communication can block all buses of the hierarchy. Network-on-Chip is a new paradigm for designing future SoCs [1] where various IP blocks are connected to the router based network of switches using resource network interfaces. The network is used for packet switched on chip communication among cores [2]. It also supports Globally Asynchronous Locally Synchronous style of implementing large chips.

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State Encoding Targeting Low Area and Low Power FSM Synthesis

Saurabh Chaudhury[1], **Krishna Teja S.**[2] **and Santanu Chattopadhyay**[3]

Abstract

The problem of assigning state codes in an FSM for minimizing the area occupied and the total power consumed i.e., the sum of the leakage power and the dynamic power in the combinational part and the sequential part of a synchronous circuit is explored in this paper. A genetic algorithm based approach is proposed targeting low area and low power FSM state assignment. The technique is applied to a set of MCNC benchmark circuits and the results in comparison with the NOVA state assignment are presented. We could obtain up to 29%, 14%, and 18% reductions in leakage power, dynamic power, and area respectively in comparison with NOVA.

Keywords: *state encoding, genetic algorithm, FSM, low area, dynamic power, leakage power.*

1. Introduction

The power lost due to leakage becomes increasingly significant as technology scales down into the nanometer regime in a CMOS chip. The main reason for this is the reduced CMOS device threshold voltage, which leads to a large increase in the device sub-threshold current. Also, as the gate oxide gets thinner, tunneling current through the insulator becomes a non-negligible component of power consumption [1, 2]. Therefore, more constraints, which necessitate an introduction of new cost functions accounting for both static and dynamic leakage along with new optimization techniques, must be introduced into a design at the system level to account for the total power dissipation. Quite a few contributions in the domain of low-power dynamic state assignment have been found in the literature [3, 4, 5 and 6]. But, none of these techniques addresses the issue of static power consumption.

In [7], a new cost function that can be used as a metric for static leakage in FSMs, as well as new techniques aimed at minimizing static leakage along with dynamic leakage was presented. In that paper, a cost function that can be used as a cost metric for static leakage in the sequential part of an FSM was introduced. But, the power consumed in the combinational part is not accounted for. In this paper, we implement of the combinational part in an FSM using PLA, to complement the work done in [7]. The new cost function for the static power in

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A POWER EFFICIENT CARRY BREAK ADDER IMPLEMENTATION USING INPUT PATTERN BASED AREA REDUCTION TECHNIQUE FOR ADDER STRUCTURES

Krashna Nand Mishra[1], Subash Chandra Bose[2]

Abstract

In this paper, we present a novel carry break addition, which exploits certain aspects of carry generation & manipulation based on the bit positions in input vectors. It takes a design methodology into consideration while implementing it in lesser area without sacrificing the performance in terms of speed and power. Selective use of certain circuit structures and transistor sizing are carefully done to result in low power design. Depending on input vectors, it shows high speed carry generation with worst-case delay of 3.23 ns for four-bit adder slice. Considering the layout regularity and circuit topology, it has been integrated into an area of 8871µm^2 in 1.2 µm 5V SCL CMOS technology. Exploiting the behavior of bit-slice architectures, 32b MCBA Macrocell has also been designed and implemented using these four-bit slices.

Keywords: Adder, Low power design, Bit-slice.

1. Introduction

Adder is one of the most widely used building blocks in all data processing (arithmetic) and digital signal processing architectures. In VLSI applications, Area and Power are very important factors that are taken into account while designing fast adders. But other than these, success of design also depends on some critical parameters like testability and ease of design. And for high performance adder implementation, Carry generation logic plays a very important role. In this work, we have analyzed carry generation & propagation logic and tried to map it to an effective transistor level circuit implementation to reduce the complexity in designing adder circuits.

In this paper, novel architecture for improved carry generation for adders will be presented and the circuit techniques for realizing different blocks used in four-bit MCBA slice using transmission gate-pass transistor based logic will be described. Section 2 lists the design methodology aspects that have been considered for transistor level implementation of the circuit. The proposed architecture for Four-bit slice has been described in section 3. The behavior and transistor level circuit implementation of different blocks used in this slice is discussed in its sub-sections. Different aspects of bit-slice implementation and its utility for the implementation has been discussed and covered in section 4.

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Area Efficient Bit-Serial Architecture for Polynomial Basis Multiplication over Galois Fields $GF(2^m)$

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Abstract

This paper presents a bit-serial polynomial basis multiplication architecture over finite fields GF(2^m). Based on the formulation of well-known Mastrovito's algorithm, we develop a generalized architecture for the bit –serial multiplier and analyze the time and gate complexities of the proposed multiplier as a function of degree m and the reduction matrix Q. The proposed architecture minimizes the number of logic gates by reusing the same hardware by cyclic shifting of one of the input operands. The proposed architecture for the bit-serial multiplier requires less area compared to the architecture presented earlier keeping the latency same.

Index Terms - Finite or Galois field, Mastrovito multiplier, cryptography, error control code, VLSI testing, digital signal processing, bit-serial, bit parallel.

1. INTRODUCTION

Finite field also known as Galois field arithmetic operations over $GF(2^m)$ find increasing applications in public-key cryptography, error detecting and correcting code [13-14], VLSI testing [15], digital signal processing [16]. There are different equivalent representations for field elements of $GF(2^m)$ e.g. Polynomial base, normal base, and dual base. We concentrate only on polynomial base (PB) representation. The two basic operations over $GF(2^m)$ are addition and multiplication. Addition in Galois fields over $GF(2^m)$ is relatively straightforward to implement, requiring at most m XOR gates. The multiplication operation is much more expensive in terms of gate count and clock cycle than addition. The other operations of the $GF(2^m)$ fields like exponentiation, division, and inversion can be performed by repeated multiplications.

Over the years, various multiplication architectures have been proposed for efficient design, such as bit-serial, digit-serial, and bit parallel. So far, various researchers presented GF multiplier design with respect to complexities, delay, power and gate count. Most of the work is focused on VLSI implementation and synthesis of *GF* multipliers. In applications where area is the main concern, serial type design is the architecture of choice which computes $GF(2^m)$ multiplication in the O(m) cycles using $O(m)$ logic elements. However, the problem with serial architectures is that its latency. To avoid the problem of time complexity, the bit parallel multiplication architectures are used. Although this architecture computes the multiplication in single clock cycle, the logic complexity is $O(m^2)$. In this paper, we propose an alternative formulation for a

A Bus Encoding Technique for On-Chip Propagation Delay Minimization

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Abstract

With the shrinking of CMOS process technology, propagation delay on long on-chip interconnects is increasing. Minimization of propagation delay becomes one of the important design objectives as large propagation delay can hurt the system performance. In this paper, by exploiting data similarity in the address/data bus data, we propose a bus encoding technique for on-chip propagation delay minimization and show that for a 1-cm 32-bit bus in 90nm CMOS technology, our bus encoding technique requires 48 wires and achieves 69% and 50% delay savings for address and data buses, respectively.

Keywords: Bus encoding, crosstalk, delay, on-chip bus.

1 Introduction

Propagation delay on on-chip interconnects depends on the interconnect features as well as the transition patterns of data that is transmitted over interconnects. As CMOS process technology scales down to nano-meter region, interconnect resistance increases with shrinking interconnect width and the coupling capacitance (C_I) increases with reducing spacing between interconnects. Also, on-chip global interconnects are increasing in length with increasing die sizes. Increase in the interconnect resistance, length, and coupling capacitance results in large on-chip propagation delay [5,17]. In addition to the interconnect features, data that is transmitted over the interconnects can also influence propagation delay as opposite transitions on adjacent wires result in high propagation delay compared to the transitions in the same direction.

As propagation delay limits the performance of the system, it is very much important to devise techniques for delay minimization. One way to minimize propagation delay is to eliminate opposite transitions on adjacent wires. Several bus encoding techniques have been proposed to eliminate opposite transitions on adjacent wires [3,6,14,15,18]. Most of the existing bus encoding techniques considers uniformly distributed random data for evaluation and hence they may not exploit the data behavior of an application.

In this paper, we propose a bus encoding technique for on-chip data transmission delay minimization. Our technique exploits the similarity in the MSB 16 bits of address/data bus data of SPEC2000 CPU benchmarks and achieves significant delay savings with few redundant wires as compared to the existing bus encoding techniques.

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A DOUBLE PULSED LATCH FLIP-FLOP

K.Navaram Kumar[1] K.D.Kulat[2] Rajendra M.Patrikar[3]

Abstract

Chip power can be divided into two main components: dynamic switching and static leakage. Dynamic power dissipation is given by P = 1/2CV ^{2}f, where C is the average total on-chip capacitance switched per cycle. Up until recently, VLSI scaling could be counted on to alleviate the power problem. Ever since the 0.5 µm generation, the gate dielectric oxide thickness, supply voltage, and threshold voltage have scaled with device dimensions by 0.7Â— per generation to limit the growth of dynamic power consumption while improving performance. The reduction of oxide thickness and threshold voltage has led to exponential increases in static leakage power. There are six leakage mechanisms in nanometer scale transistors, of which the three most significant are sub threshold leakage, gate leakage, and band-to-band tunneling (BTBT) leakage

In digital circuits flip-flops are critical timing elements and have a large impact on circuit speed and power consumption. Power consumption is primary challenge in deep submicron technology, as the number of transistor goes on increasing on die leakage current is also increases and thus static power consumption also increases. Lot of work has been done to develop fast and low-power flip-flops. Minimum D to-Q delay is the primary measure of a flip-flop, as this determines how much impact the flip-flop has on cycle time. By reducing the transparency period of a latch to a narrow window, the latch can operate as a flip-flop with the additional advantage of allowing limited time borrowing across cycle boundaries to reduce sensitivity to clock skew and jitter. The pulse generators can also consume considerable energy, as pulses must be generated locally to avoid pulse distortion. Nonetheless, because of their performance advantages, these pulsed latch structures have been used in several commercial high performance digital systems. Apart from raw performance and energy consumption, other attributes are used to evaluate flip-flop structures including robustness.

A new flip-flop design using a double-pulsed static latch is designed for 65-nanometer technology where leakage power is dominant. This flip-flop consumes less power and fewer transistors in the pulse generator as compared with the DPSCRFF (Double Pulsed Set Conditional Reset), which is one of the fastest known flip flop in literature. The double-pulsed latch flip-flop avoids unnecessary switching, and stacking of transistors. Because of these design features this flip-flop consumes less dynamic power and less static power. A pulse generator is important part of the new types of flip-flops. A pulse generator is modified to suit the circuit, which generates less width pulses in turn this increase the maximum clock frequency

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DESIGN OF FLIP-FLOPS WITH LOW SETUP AND HOLD TIMES ACROSS PROCESS VARIATIONS

Pratap Kumar Das[1], Bharadwaj Amrutur[2], J. Sridhar[3]

Abstract

In this paper we investigate the impact of process fluctuations on the variability of the set-up and hold times of flip-flops. A set of flip-flops available in the literature are discussed in the context of low uncertainty window for sampler type of applications. We find that differential sense amplifier flops show less variability than single ended ones, due to the inherent properties of the differential structure. We suggest a simple technique to generate a built in reference for a differential flop, which enables its application in single ended digital type applications, but still preserves all the robustness properties of a fully differential structure. We have evaluated the flops in an industrial 65nm process and simulation results show that our proposed flop has around 5X reduction in its uncertainty window compared to a single ended standard master slave flop, as well as about 2X reduction in the variations in the window across process corners. Our proposed structure also maintains almost constant uncertainty window over the supply voltages from 1.1V to 0.8V unlike the single ended flops.

Keywords: Samplers, Variability, Sense Amplifier, Flip-flop.

1. Introduction

Samplers [1] or flip-flops are integral elements of any digital system and with technology scaling down and increasing clock speed, the non idealities of the flip-flops are becoming more important. Some of the important design parameters of the flip-flop are the setup time, hold time, power and the clock to output delay [1] which affect the latency and the speed of the over all system. But when the samplers are used to capture data which is asynchronous to the sampling clock, the timing parameter of interest is the sum of the setup and hold times i.e. the total uncertainty window given as $\tau_{setup\text{-}hold} = \tau_{setup} + \tau_{hold}$ [1]. In such applications, not only should the uncertainty window be small, its variations due to process fluctuations across a chip should also be minimized. With scaling into deep submicron technologies, the process parameter variations are expected to increase and hence one can expect larger variations in circuit operation. In this work we study the impact of process fluctuations on the

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A Novel Approach for Power Pad Layout generation

Venkat Rao Vallapaneni[1], Sireesha L. N. V. S. Tulluri[2], Srinivasarao Gandi[3] and Raghunatha Reddy Lakkireddy[4]

Abstract

The on chip power demand is met through the external power sources. These external sources are connected to the internal power rings through pad pin and metal bussing of the power pads. Pad pin provides connection to the bondpad, which is a wire bonding location. Layout views for Power pads are required for the floor-planning step in the physical design stage. Since the Power pads and IO buffers interface with robust external world, protective devices are employed. These protective devices are analog in nature and hence require special techniques while creating their layout views. Normally, the layouts for power pads are done manually taking area and robustness into consideration. In this paper, a novel approach is proposed for automated layout generation of a power pad. It consists of two stages, i) Cost effective placement of the protective device layout on the bus frame. The placement cost is dependent on routing costs and overlap areas. ii) DRC (Design Rule Check)-clean connection of both pad pin and protective device power/ground with the respective supply busses in the frame. The resultant connections are robust and match manual routing. Due to automation, layouts are generated much faster (25X improvement) and human errors can be minimized. The proposed router is generic and thus can be used for various types of power pads and can be easily migrated to the newer technologies.

Keywords: Power pads, layout, corner-stitching, minimum spanning tree

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POWER SUPPLY DETECTION CIRCUIT

Dharmaray Nedalgi[1] and **Mukesh Nair**[2]

Abstract

In an integrated circuit (IC) for low power applications, power down mode (suspend mode) is widely used concept for power saving. In power down mode, core supply is switched off to portion of the core logic which is not operating, whereas the external supply is still on. The bridging of core and external voltages is done in an interface (I/O) circuit. In the absence of the core supply, the state of the level shifter in I/O circuit is not defined. The undefined state of level shifter circuits may lead to leakage in external supply and also the wrong signals to the receiving IC which might cause functional failure. It is necessary to put the level shifter circuit in defined state during core power down mode.

In this paper we report a low power; supply detection circuit to identify the core power down mode. The main features of this circuit is, use of the dynamically configurable blocks to provide positive feed back to speed up the supply level detection process both during power up and power down modes. This circuit has inbuilt hysteresis which ensures the reliable switching from power down mode to power up mode and visa-versa. This circuit has almost negligible static current. This supply detection circuit operates for wide range of external supply voltage without re-design, which makes it compatible to use in many applications. This circuit is designed to detect the core supply voltage as low as 1.0 volt (nominal), while external voltage is varied from 1.65 volts to 3.6 volts. This circuit is implemented and qualified on silicon on 0.18um CMOS technology. This circuit is portable to advance technologies like 0.13um, 90nm and 65nm technology.

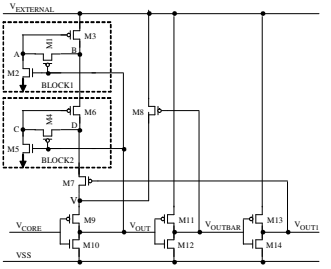

Figure 1: Proposed power supply detector circuit

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VCO PHASE NOISE IMPROVEMENT TECHNIQUES

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Eapen Abrahim: Cornet Technology India

Abstract

A 3-stage CMOS Ring Oscillator with replica bias is implemented in 0.18µ TSMC technology. The Proposed modification for the existing architecture shows Phase Noise (PN) improvement about 6dBc at 1 MHz offset. Oscillator core current consumption, tail transistor voltage variation (VDS) and Phase noise performance across 3 corners have been tabulated in table1. The Phase Noise measured with proposed modification was –106dBc/Hz @ 1 MHz offset for 500 MHz operating frequency.

Keywords: Ring oscillator, CMOS VCO, Replica Bias

1. Introduction

Voltage controlled oscillators (VCO's) are essential building blocks of modern communication systems. The VCO performance in terms of phase noise, tuning range, and power dissipation determines many of the basic performance characteristics of a transceiver. Designing VCO with better PN has always been most desirable and most challenging. In this paper an attempt has been made to improve the phase noise performance with little modification of the existing architecture.

2. Base VCO Design

Most basic CMOS ring oscillator employ odd no of delay cell as shown in fig. 1. [1]. The figure also shows replica bias followed by CCO and differential to single ended converter at the end. The architecture of the delay cell used in VCO is as shown in fig.2.

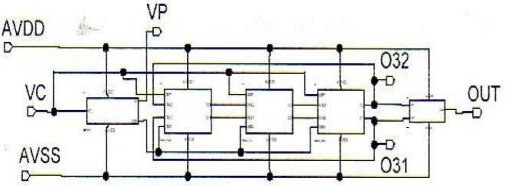

Fig.1. 3-Stage CMOS Ring Oscillator with replica bias

DEVELOPMENT OF AN FPGA BASED SMART COMPUTING SYSTEM FOR CLINICAL DIAGNOSTIC APPLICATIONS WITH ON-BOARD WIRELESS COMMUNICATION FACILITY FOR REMOTE TRANSMISSION OF CRITICAL PATIENT DATA

Authors: Shubhajit Roy Chowdhury[1], Hiranmay Saha[2]

Abstract

The recent integration of soft computing techniques with VLSI reconfigurable architectures has motivated the development of a smart diagnostic system for renal therapeutic applications. The paper describes the FPGA implementation of a smart diagnostic system that uses fuzzy logic techniques to predict the physiological state of a patient. The diagnostic function realized on the FPGA based smart system has been suitably integrated with a wireless communication chip on board to facilitate remote communication of patient data as is required in telediagnostic environments. Instead of a more optimal ASIC based implementation, FPGA chip is chosen for implementation purposes mainly for its low design cycle testing and its performance is found to be satisfactory. The system employs a smart agent that can predict the future pathophysiological state of a patient using the past pathophysiological data and can thus predict the approaching critical condition of the patient before criticality actually occurs. This feature has been implemented using fuzzy logic. The smart processing system consists of blocks for fuzzification, inferencing and defuzzification of patient data. In order to save the number of combinational logic blocks in implementing the system, the division process required for normalization of membership functions is implemented using intelligent multiplication techniques. In order to speed up the computation process, pipelined data processing architectures have been employed leading to a speed up of approximately 3.11. The smart system is realized on Altera Cyclone EP1K6Q240C8 FPGA chip requiring approximately 5,308 logic blocks. To facilitate remote communication of the patient data, the output ports of the FPGA chip has been suitably interfaced with wireless communication chip CC2500 that supports data communication at speeds of 2.45 GHz. The maximum power dissipation of the system is estimated to be about 642.3mW.

Keywords: FPGA, fuzzy logic, pathophysiological, diagnosis

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Strategies for Power Reduction during VLSI Circuit Testing

Santanu Chattopadhyay[1]

Abstract

With the increasing use of battery-operated low power devices, a newer challenge has come up to the test engineers to ensure that the circuits do not consume much power in the testing phase as well. To keep the test power budget low, several modifications have been proposed in each and every aspects of VLSI testing. This includes modifying the test generation algorithms, internal and external testing, DFT and BIST architectures, modifications in the scan chains, and so on. This embedded tutorial gives an overview of these strategies proposed in the literature.

Keywords: VLSI testing, low power testing, low power ATPG, low power internal testing, low power external testing.

1. Introduction

Testing bridges the gap between the imperfection of manufacturing process for integrated circuits (IC) and the end user's expectations of defect-free chips. Manufacturers test their products to discard the faulty components to ensure that only the defect-free chips make their way to the consumer. With the advent of deep sub-micron technology, the tight constraints on power dissipation of VLSI circuits have created new challenges for testing low power VLSI circuits which need to overcome the traditional test techniques that do not account for power dissipation during test application. Since much of the power consumed by the circuit is dissipated as heat, the relationship between the test activity and the cooling capacity need to be taken into consideration in order to avoid destructive test. Moreover, many of the mobile devices in use are hand-held, battery-operated, and plastic packaged. Criticality of their operation often needs periodic testing of these equipments. Thus, test power reduction becomes one of the major issues to ensure long battery life, low heat dissipation, and lighter packaging.

This tutorial aims at illustrating the alternative avenues to reduce the test power. In particular, the following aspects will be covered.

- Importance of test power reduction
- Ad-hoc industrial solutions and their short-comings
- Power minimization in internal testing using BIST and it's modifications
- Power reduction in external testing via
    - test vector ordering

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Design and Simulation of Integrated VCO for SMART Nanoporous Silicon Based Biosensors

Abstract:

Design and simulation of a ring oscillator based all NMOS voltage controlled oscillator (VCO) integrated with a nanoporous silicon based biosensor is presented in this paper. The integrated sensor offers the advantages of improved noise immunity, better resolution and low power consumption crucial for biosensing applications. To perform the integrated design and simulation, a SPICE compatible model of the biosensor has been developed based on experimental results which has been linked with the VCO using the dynamically linked library of the SPICE simulator. The biosensor is modeled as a distributed RC diode network with a lumped equivalent parallel RC network the biosensor forms as depicted by the CV measurement. The impedance of the biosensor which has been designed for sensing the status of dehydration changes with the sodium ion concentration or osmolality of the body fluid of the patient which ultimately changes the oscillation frequency of the oscillator. The optimum frequency of operation of the VCO is chosen to be around 250kHz since the Q factor of the biosensor capacitor is also highest at this frequency thus resulting in a lower harmonic distortion of 5.393% and phase noise of –95.46dBc/Hz at 100Hz offset frequency in the VCO output. The VCO is designed using BSIM V3.0 0.8µm technology with 3V supply and at a dc bias of 10mV. The oscillation frequency is found to vary from 260kHz to 390kHz with the change in osmolality from 40 to 400 corresponding to low, moderate and highly critical dehydration state of the patient.

1. Introduction:

Since the development of silicon microsensors, there has been consistent effort to integrate the sensor with MOS circuits to lead to integrated sensor system. K.S.Wise had demonstrated the first integrated pressure sensor [1], which was implanted in the catheter tube of a patient. There are also other contemporary reports of integrated inertial sensors [2,3]. Such integrated sensors offer the advantages of improved noise immunity, better resolution and low power consumption making them suitable for field use. Recently there are reports on the implementation of complete microsensor system for continuous monitoring of ions, dissolved gases and biomolecules [4, 5], which are used for improvement of critical, care patients in intensive care units. In this paper we report the fabrication and testing of ordered porous silicon based dehydration sensor. A lumped electrical model of the sensor is also developed based on the experimental results where the dependence of the parameters of the model on the dehydration conditions of the solution is estimated empirically. The model is then linked with a ring oscillator based MOS VCO to detect the change in impedance to the change in frequency of the VCO. The VCO is designed using 0.8µm technology.

Dehydration is one of the commonest paediatric medical problems leading to significant mortality and morbidity and economic burden on the health care services.15 to 40% casualties below the age of five years are due to dehydration caused by diarrhoeal diseases. The instruments available for measurement are either expensive or invasive in nature and hence are not suitable for field use in the rural areas [6,7]. Thus development

Dcache and Icache Memory Testing Using CPU BIST

Sourabh Saluja [1] and Vijay Sindagi [2]

Abstract

The SoCs targeted for critical applications such as automobile and medical etc. have extremely low DPPM requirements. So it becomes imperative to test each part of the design rigorously. The failure analysis from previous projects in Texas Instruments (TI) shows that most memory failures occur due to faults in metal interconnects. Based on this study, a set of memory testing algorithms has been developed by TI experts to cover all known faults. In a simple, directly addressable memory block, the implementation of these algorithms is straightforward. But in case of cache, problem becomes compounded because it depends on the cache architecture that how many blocks are present and in what order the words are stored in those blocks. It becomes even more complex in case of instruction cache as we cannot choose just any pattern -- it has to be a valid instruction code. There are other challenges as well with cache testing. This paper discusses our strategies for Dcache and Icache testing for ARM926EJ-S, which was a part of an SoC for automobile applications.

Keywords: CPU BIST, Cache Testing, SoC, ARM

1 Introduction

1.1 Problem Description

Lately, there has been a great emphasis on memory testing. More so due to:
a. Memory faults being reported mainly due to metal interconnect defects and inability of current BIST tools to address these defects.
b. Extremely low DPPM (Defective Parts Per Million) requirements in the devices targeted for critical applications like Automobile, Medical etc.
c. Lessons learned from previous projects. For example, in case of one System-on-Chip (SoC), there was fallout of up to 4 out of 16 memories. It had severe repercussions like:
(i) TI had to ramp this product to volume production with a low yield.
(ii) It took several staff months to resolve the issue.
(iii) TI had to release a partial PG (tape-out) to get back to a profitable product.

In the past, the memory circuit designs might not have been characterized to the degree necessary to guarantee against all failure mechanisms, the main reasons being:
a. Embedded memories are built in a process optimized for high-speed digital logic

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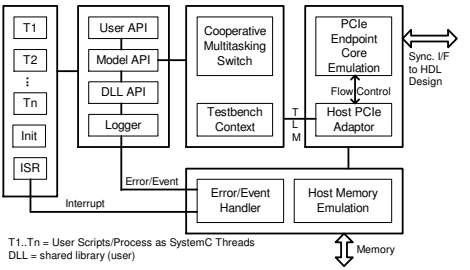
Co-simulation: Verification Advantage with PCI Express Endpoint SystemC Model

Aditya Ayre[1], Aniket Deshpande[1], Vishal Rustagi[1]

Abstract

Functional verification of a Network Processor design requires a simulation environment that emulates a generic host-system. The emulation involves multiple processors, direct memory access, interrupt service routines (ISR), exceptions and error handling, synchronization objects, etc. Additionally, the Network Processor (providing the transport layer) specific driver support involves special data-structures, programmed I/O, block memory transactions. Our design of Network Processor, in Hardware Description Language (HDL), uses PCI Express (PCIe) interconnect module (an Endpoint core from third-party). We have developed a replacement simulation-model using restricted-use of SystemC (to improve simulation speed). Besides these requirements, its additional aim was to reduce overall simulation speed bottlenecks, simplify testbench creation (independent of programming language, e.g. C/C++), integrate testbench module within the design itself (by replacing Endpoint Core, and concentrate not on testbench creation but on testcases). The high-level architecture of the model is shown below.



This eliminates the need for two back-to-back instances of PCIe Endpoint Cores and additional testbench creation in HDL. The improved overall simulation speed (by factor of ~10) and reduced memory usage (by factor of ~5.5) results are quite encouraging to apply same model to verify other designs having similar interconnect. The testbench complexity was transferred from HDL to external processes enabling efficient test-suite development for simulation.

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Case Study: Reducing Run time of Volume Diagnosis by Using Reduced Pattern Set and Truncated Failure Log

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Diagnosis is performed to localize the defects which exist inside the faulty devices. The diagnosis process requires ATE failure data, the structural test vectors and the design. The time spent by test engineers for diagnosing the faulty devices does increase with the growing complexity and shrinking feature size of the design. Hence, for reducing the diagnosis time in volume production, there is a need to limit the applied pattern count and restrict the size of the failure data, without affecting the diagnosis resolution. This paper presents an approach for successful detection of bridging faults using the reduced pattern set and re-arranged failure log data. Experimental results based on three industrial designs are also presented to demonstrate the effectiveness of the proposed method for volume diagnosis.

1. INTRODUCTION

The ATE *(Automatic Test Equipment)* logs the failing device information in either of the ways: It uses a centralized buffer to log the failing cycles or it uses the dedicated per pin based buffer to log the information of the failing cycles. In the second approach each pin can reach the maximum logging capacity independent of the other pins on a failing chip. [1] As diagnosis is a post-silicon process, the time required by a volume diagnosis tool to successfully diagnose the failing devices depends on two main factors: the number of relevant test patterns and the number of failing cycles logged by ATE.

In a 4-way bridge fault model [2] the bridging behavior might be seen in those lines which are physically closer to each other in the layout. Figure 1 shows a 2-input AND gate. A dominant node might drive the victim node. For instance, a HIGH value at node A (dominant node) might drive a HIGH value at node B (victim node) when the original value at node B was supposed to be LOW. In the same manner there can be four such possible combinations for a 2-input AND gate. These combinations are listed in Table 1.

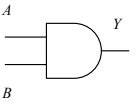

Figure 1: 2-Input AND gate

Dominant Node	*Victim Node*
A = 0	B = 1 → 0
A = 1	B = 0 → 1
B = 0	A = 1 → 0
B = 1	A = 0 → 1

Table 1: 4-Way Bridge fault model

Formal Verification of a Fast DMA Controller: A case study

Bijitendra Mittra[1], Subir K Roy[2], Anindyasundar Nandi[3], Prohor Chowdhury[4]

Abstract

This paper presents a detailed description of the application of formal verification methodology to verify an implementation of a multi-channel fast DMA controller. The controller uses features such as read-write pipelining, arbitration and priority schemes, address pointers calculations, transfer control logic and interrupt and synchronization handling. It is a well-known fact that verification with formal methods works best at the module or block level. With increasing design complexity, application of formal methods become even more limited and do not scale well at the full chip level. In this paper, we share our experiences about applying formal verification methodology both at the block level as well as top-level. We also discuss the advantages and disadvantages of both the approaches in comparison with conventional verification methodology. We compare the runtime statistics of both the approaches and show that applying formal verification at the top-level can be useful depending on the design complexity. We present data to validate the proposed approach. Our approach was successful in finding two corner case bugs missed out by the simulation team despite having a stringent process centric review of testplan generation and test validation.

1. Introduction

In this paper, we present our experience of verifying a fast DMA controller using formal verification vis-à-vis it's simulation-based verification. We discuss two different approaches taken to verify the design and the advantages and disadvantages concurrently. The formal verification effort was carried out in parallel with the simulation-based verification with the prime objective of complementing the verification process to ensure quality and robustness. The first approach taken to formally verify the controller was to do an end-to-end verification at the top-level. Hitting a bottleneck with the runtime of the properties at the top-level, it was decided to do a compositional verification on the design and run it at the block level first. Finally, we came back to applying the top-level approach once again to check the completeness of the block-level approach. Due to the highly proprietary nature of the details of the design and specifications, we primarily focus on the methodology, techniques and experience involved during the verification process.

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POWER OPTIMIZED MACHINE CODE GENERATION FOR APPLICATION SPECIFIC INSTRUCTION SET PROCESSOR (ASIP) FOR HINDI TEXT TO SPEECH SYNTHESIS

Sanjay Singh*, A. S. Mandal

Central Electronics Engineering Research Institute, Pilani.
* Student Trainee, Kurukshetra University, Kurukshetra.

In the past, performance and area were the key parameters in the processor design. In response to this demand, Computer-Aided-Design (CAD) tools were developed to automate the design process for achieving maximum speed and minimum area. Recently, the portable consumer-electronics (battery-operated products) market entered a period of explosive growth. At the same time, the amount of data to be processed is increasing at a rapid pace. This calls the faster digital devices, which in turn increases the power consumption that causes packaging and reliability issues. These considerations have resulted in a growing need for minimizing power consumption in today's electronic systems. In this paper, we explain the process of power optimized machine code generation for ASIP for Hindi TTS synthesis. Power consumption is reduced by minimizing the switching activity on the data & address bus lines of ASIP. The switching activity minimization is done by using the low power address assignment methodology for integer memory parameters, floating point memory parameters, & instruction opcodes. Then instruction reordering is used to minimize the switching activity of the program memory. By using these techniques, the resulted power reduction for ASIP bus lines is ***20.165%****. The final voice output is obtained.*

1. Introduction

From human prehistory to the new media of future, speech communication has been and will be the dominant mode of human social bonding and information exchange**[6].** Synthetic and artificial speech has been developed steadily during the last decades. In 1980 Dennis Klatt proposed a complex formant synthesizer which incorporated both the cascade and parallel synthesizers with additional resonances and anti-resonances for nasalized sounds, sixth formant for high frequency noise, a bypass path to give a flat transfer function, and a radiation characteristics. He successfully implemented the PC-based TTS converter for this system in FORTRAN (1980) and then in C**[7]**. The growth of portable devices consumer electronics market motivated the hardware implementation of the TTS converters. The TTS converter has two parts text analysis and synthesis. The text analysis part (rule chip) analyses the text and generate the phonetic information using some rules. The synthesis part (voice chip) converts the phonetic information into speech. Limiting our first attempt, for hardware implementation of TTS converter, to our home country, we are designing the ASIP for HINDI text-to-speech conversion at IC the Design Group, CEERI, Pilani, using Klatt's C code as the starting point for the synthesis part (voice chip). The block diagram of ASIP for HINDI text-to-speech conversion is shown in Figure 1.

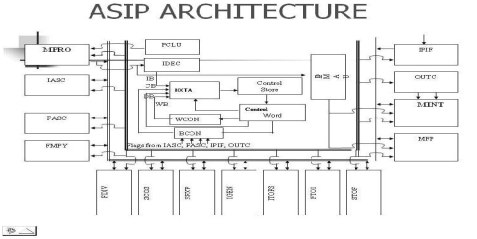

Figure 1: Block Diagram of ASIP.

Implementation of SPIHT Codec In Stratix-II

Kishore B.[*], Ramesh K.S.[*], Mate G.V.[*], Anbuselvi J.[*]

Abstract

A combination of Discrete Wavelet Transform DWT (which is lossless) plays an important role in image compression and Set Partitioning in Hierarchical Trees SPIHT coding (known for higher compression ratio with restoring quality) is used for our implementation. In this paper, we presented an implementation of the image compression routine SPIHT algorithm in reconfigurable logic. Among several architectures and methods we selected (Daubechies 9/7-tap filter) lifting scheme for DWT implementation and SPIHT codec is implemented with popular algorithm proposed by Amir Said and Pearlman [1].

A general-purpose hardware has been designed and developed for image/video compression. In this, image is grabbed through a camera and it is compressed using SPIHT algorithm and on the compressed image the decompression algorithm is applied and the resultant image is displayed on the VGA monitor. Several interfaces like LAN, USB, Remote Control, RS232, Modem, LCD, IRDA, Keyboard and Mouse are provided on the board in order to enable it for different applications.

This paper concentrates on the implementation of SPIHT codec and it is tested for LENA image of the size 128x128 with different compression ratios and PSNR. The Altera Stratix-II device has been targeted for this implementation.

Keywords: SPIHT, Compression

1. Introduction

The huge amount of information included in the picture makes its high utility value but unfortunately causes necessity of wide band transmission channels. For example, in this digital era, people use internet to download images but they have to wait for the sufficient image to be received to confirm if this image is necessary or not. In that case they have to pay high for both time and money due to insufficiency of the bandwidth and the traffic jam of the network. Image compression has been playing key role for the applications, which depend on the efficient manipulation, storage, and transmission of binary, gray scale, or color images. Therefore, systematic design of an image compression system with restoring image quality is required. Conventional wavelet based image codec like SPIHT yield excellent result and create embedded bitstreams.

In this paper, SPIHT codec is implemented in reconfigurable logic. Selection of the submodules used for implementation made by keeping in mind to achieve good image quality as well as high compression ratio. Initial sections will

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FPGA Implementation of Low Power ASU Multiplier

Rahul M Badghare[1], Sanjiv Kumar Mangal[2], Raghvendra B Deshmukh[3], Rajendra M Patrikar[4]

Abstract

In the fast growing mobile communication devices, requirements of low power designs are increasing to reduce the power losses and decrease the thermal hot spots. Also various digital signal-processing chips are now designed with low power dissipation. Thus the architectures which are suitable for FPGAs also are preferred for implementations in a system. Multiplier is an arithmetic circuit that is extensively used in common DSP and communication applications which exhibit high degrees of parallelism. In this paper we have presented low power multiplier design methodology that not only inserts more number of zeros in the multiplicand but also uses a special design adder-substractor circuit to achieve more power reduction. The number of zeros that can be increased in the operand is discussed with the help of Binary / Booth Recoding Unit. As we know that the switching activity of the component used in the design depends on the input bit coefficient. This means if the input bit coefficient is zero, corresponding row or column of adders need not be activated. If operand contains more zeros, higher power reduction can be achieved. Proposed Binary / Booth Recoding Unit will force operand to have more number of zeros and it becomes more efficient for higher width of the multiplicand. Also special designed adder-substractor unit avoids extra addition circuitry needed for2's complement operation in booth multiplier and hence contributes to less reduced switching activity. In order to evaluate the performance of low power ASU multiplier, we implemented all designs on Xilinx xc2vp2-6fg256 FPGA. We compare the performance of this design with column bypassing multiplier, row bypassing multiplier and multiplier without bypassing. The results obtained clearly indicated that our method could save the power even in an implementation on FPGA. It clearly indicates that booth-recoded multiplicand saves significant amount of switching activity as compared to the binary multiplicand. Use of look up table to count the number of one's is an added feature to this design that makes it suitable for FPGA implementations also.

Keywords: Low Power, FPGA, Multiplier, Switching activity, Binary / Booth Recoding Unit, Adder-Substractor Unit

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Improved Reversible Logic Implementation of Decimal Adder

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Abstract

In recent years, reversible logic has emerged as one of the most important approaches for power optimization with its application in low power CMOS, quantum computing and nanotechnology. An improved design for a reversible logic implementation of Binary Coded Decimal (BCD) adder is proposed in this research. This design not only reduces the number of gates and garbage outputs compared to the existing BCD adder reversible logic implementations, but also suggests a better logic implementation. So, this design gives rise to an implementation with a reduced area and delay.

Keywords: BCD adder, decimal arithmetic, reversible logic, low power designs

1. INTRODUCTION

Energy loss during computation is an important consideration in low power digital design. Landauer's principle states that a heat equivalent to *kT*ln2* is generated for every bit of information lost, where '*k*' is the Boltzmann's constant and '*T*' is the temperature [1]. At room temperature, though the amount of heat generated may be small it cannot be neglected for low power designs. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Bennett showed that energy dissipation would not occur if the computations were carried out using reversible circuits [2] since these circuits do not lose information. Information is lost when the input vector cannot be uniquely recovered from the output vector. The gate that does not lose information is called reversible gate. For such circuits there is a one-to-one mapping between input and output vectors. A reversible logic gate is an *n*-input, *n*-output (denoted as *n*n*) device that maps each possible input pattern to a unique output pattern. There is a significant difference in the synthesis of logic circuits using conventional gates and reversible gates [3]. While constructing reversible circuits with the help of reversible gates fan-out of each output must be 1 without feedback loops. As the number of inputs and outputs are made equal there may be a number of unutilized outputs in certain reversible implementations. The unutilized outputs from a reversible gate/circuit are called "garbage". This is the number of outputs added to make an n-input k-output function reversible. For example, a single output function of 'n' variables will require at least n-1 garbage outputs.

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Modified Data Encoding Circuit for Asynchronous FIFO Design

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Abstract

A multi-valued logic data encoding circuit with lower switching power consumption is realized. In an asynchronous design, a conventional ternary encoding makes all data lines change to intermediate values to indicate the completion of data signal. Similarly, in RT/NRT encoding, the data lines transferring "1" will always change to intermediate value. In the proposed modified RT/NRT, not all '1's are transited to intermediate value. Only the first '1' of data is changed to intermediate value and thereby decreasing the number of transitions and switching power compared to RT/NRT encoding. Multi-valued logic data encoding circuit for ternary (circuit 1), RT/NRT (circuit 2), and the proposed modified RT/NRT (circuit 3), are designed. These circuits are implemented in HSpice using 90nm technology devices.

Frequency of data transmission for circuit 1 is varied from 1000ns to 3ns with 50% duty cycle. The propagation delay of the data encoding circuit obtained was from 0.7ns to 1.5 ns and on an average, the propagation delay is about 0.93ns. Almost no error was obtained at low frequencies, but at 1 GHz, an error of 21% from the desired value was occurred. The average power consumption of the data encoding circuit is 178µW/3bits.

Similarly, for circuit 2 also frequency of data transmission is varied from 1000ns to 1ns with 50% duty cycle. The propagation delay of the data encoding circuit varied from 0.6ns to 1.5 ns and on an average, the propagation delay is about 0.9ns. The error rate has been increased in this case with a value of 0.126% at T=1µs and 50% duty cycle. An error of 20% at T=1ns is observed. The power consumption of the data encoding circuit is 158µW/3bits.

For circuit 3, the individual components are verified separately and the entire circuit is tested with T=1ns and output is almost error free. For an input of [1,1,1] the output obtained is [$\frac{1_{DD}}{2}$,1,1] as expected. However, the average power consumption of this case is more (239µW/3bits) than RT/NRT circuit due to circuit complexity. Nevertheless, a separate calculation of the switching power component resulted in 25.76% lower value in modified RT/NRT, compared to RT/NRT. The circuit complexity and the total power consumption are the limiting factors of the proposed scheme. The proposed circuit can be used in any general handshaking scheme especially when less number of transitions are desirable.

Keywords: Asynchronous, FIFO, ternary encoding, RT/NRT encoding

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Design and Simulation of a CMOS Instrumentation Amplifier for signal conditioning of MEMS based Piezoresistive low Pressure Sensor

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Abstract

Possible use of ASIC chip has motivated the rapid development of low cost signal processing circuit for signal conditioning of silicon-based micro-sensors. Such signal conditioning circuits can enhance the functionality of micro-sensor system by means of amplification, lead compensation, A/D conversion, on-chip calibration and fault diagnosis. Such circuits have to operate with low noise so that they can be suitably employed in highly sensitive applications. The current work investigates the design and simulation of low noise instrumentation amplifier for amplifying the output signal of typical MEMS based piezoresistive low-pressure sensor. A survey of the contemporary literature yields different techniques of noise reduction [1] such as selection of circuit topology and device sizing. AZ and CHS have also been reported [2]. AZ reduces the 1/f noise at the cost of an increased noise floor due to sampling. CHS gives rise to residual dc components. All these external techniques are complex and increase the silicon area on chip and hence are costly. The current work aims at the development of a low noise instrumentation amplifier that provides a low cost solution to the technology requirements. The instrumentation amplifier also provides for compensation of lead resistances through intelligent circuit design techniques. Specially designed two stage low-noise operational amplifier has been used for instrumentation amplifier [1,3]. Resistances have been designed using CMOS pass transistor resistors in order to have an economy of design in respect of area of circuit as well as power dissipation. The designed instrumentation amplifier can sense the output signal of low-pressure sensor that can sense pressure in the range of 0 to 500millibar and indicate a change of 0.1mv for a change of 1millibar in the ambient pressure. The instrumentation amplifier designed in the current work has a maximum gain of 100.

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Effect of Inductance on Wire-Sizing the Global Interconnect in VLSI Circuits

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Abstract

Interconnect plays an important role in deep sub micrometer very large scale integration technologies. In this paper, the effect of inductance on the propagation delay of RLC and RC interconnects based on analytic and simulation experiments are studied. Previous research has neglected the output parasitic capacitance of the driver and the skew effect of the input waveform. We have considered the output parasitic capacitance and skew effect of input waveform to calculate the propagation delay. It is shown that the error in propagation delay between RC and RLC model increases with wire sizing. Thus, the importance of inductance in high performance VLSI design methodologies increases as the wire size increases.

Keywords: *CMOS driver, propagation delay, wire sizing, high performance, VLSI.*

1. Introduction

In current deep sub micrometer very large scale of integration circuit, the interconnect delay dominates the gate delay. This behavior is expected to increase with the continuous scaling of technology and increased die area. For deep sub micron interconnect (DSM), on-chip inductive effect arising due to increasing clock speeds, increasing interconnect length and decreasing rise times are of great concern for overall interconnect performance (E.E. Davidson et al, 1998). For global wires inductance effects are more severe due to lower resistance of these lines and also due to significant mutual coupling between wires resulting from longer return path (A. Deutsch et al, 1999). As a result, the reactive component of the wire becomes comparable to the resistive component of the wire. Furthermore, with the recent adoption of copper as the very large scale integration interconnect metal (C.F. Tsang et al, 2003), (M. Fayolle et al, 2002), line resistance has decreased and as a result inductive effect have become more prominent. Consequently, the traditional distributed RC model of interconnect especially for the global wires, may no longer be adequate since it can result in substantial error (A. Deutsch et al, 1997) while determining the propagation delay.

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CIRCUIT PROSPECTS OF DGFET: A VARIABLE GAIN DIFFERENTIAL AMPLIFIER WITH CURRENTMIRROR LOAD

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Double Gate(DG)FET is one of the most promising devices for sub-50 nm technology. The main idea of a double gate MOSFET is to have a Si channel of very small thickness and to control the Si channel by applying gate contacts to both sides of the channel. This helps to suppress short channel effects and leads to higher current as compared with a MOSFET having a single gate. Various attempts have been made to exploit this newly emerging technology in electronic circuits. In this paper an attempt has been made to explore the circuit prospects of this emerging device. I_d-V_{fg} (drain current vs frontgate voltage) curves of a DGFET were simulated in DESSIS, a commercial device simulator of ISE-TCAD package, for the device dimensions for the fabricated device [1], the device topography and doping profiles were defined in MDRAW of ISE-TCAD package. The I_d-V_{fg} characteristics were validated against that of a fabricated device [1]. This validation was done to obtain DGFETs with standard drain current vs frontgate voltage characteristics. A differential amplifier with currentmirror load was designed using the validated DGFETs. The designed differential amplifier was found to operate at supply voltages as low as 0.2 volts. A number of transient simulations were run in Dessis simulator with a sinusoidal input voltage of magnitude 1 mV for different backgate bias voltages and the corresponding gains were noted from the obtained transfer curves. It was found that the amplifier was giving maximum amplification at a backgate bias voltage of 1.3 volts for the p-channel DGFETs. With a front gate dc bias of 0.2 volts for n channel DGFETs of the differential amplifier, varying back gate bias in steps of 0.1 volts from -0.7 volt to -1.1 volts the amplifier gains were noted again and the maximum gain of 17.3 dB was obtained at a backgate bias of -1.0 volts for the n-channel DGFETs. The threshold voltage of a DGFET depends on the back gate voltage of it [1]. Now as the drain current of a short channel device depends on the threshold voltage in a nonlinear fashion [1], the transconductance of a single DGFET also depends on the threshold voltage and hence on the backgate voltage of the DGFET. Therefore, the gain of a differential amplifier designed using DGFETs is also expected to vary with the back gate voltage of the DGFETs. The important property of sensitivity of voltage gain of the designed differential amplifier to the changing back gate bias is explored hence. This feature can be used in designing automatic gain control amplifiers.

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Embedded Tutorial: Addressing Test Power Issues in Digital CMOS Circuits

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Abstract

Test power concerns are today becoming a very important component of the IC design and test cycle, affecting various aspects ranging from power grid design to packaging to tester choice. It is well known that the average power consumed during test can be 2X to 5X or more, when compared to functional power consumption. Furthermore, increased switching activity during test results in serious IR drops that can cause normal chips to be classified as fails, resulting in low yields. Technology scaling, customer requirements such as field test, etc., are ushering in additional challenges (e.g,. glitching and static power concerns, thermal issues, reduced bounds on allowed test power) that are now elevating test power to be as significant a consideration as other test dimensions (coverage, test volume, etc.)!

While test power is a well-researched problem, significant gaps exist in translating these efforts into feasible solutions that can address existing and emerging test power issues in billon-transistor chips. This embedded tutorial will highlight the test power concerns faced by IC designers, the requirements that it imposes on DFT, ATPG practices and power analysis tools, survey state-of-the-art solutions developed in both academia and industry, identify the gaps between available solutions and requirements, and summarize the open problems that needs to be addressed.

Keywords: *Testing, VLSI, Power Consumption, Test Power, IR drop, DFT, ATPG*

1. Rising Test Power Concerns

With technologies scaling to 65nm, 45nm and lower, power dissipation concerns are coming to the forefront of digital CMOS circuit design [1,2]. These concerns exist in various modes of circuit operation including functional and test modes. There are several reasons why test power concerns are dominating the thinking of IC designers even early in the design cycle:

- The power consumption requirements of a circuit in different modes of circuit operation can be different (see Table 1). Normal test mode power has already been callibrated to be several times more than functional power in existing designs, and is only expected to worsen [4,5]. While normal test mode's power consumption limits are usually around 2X functional power, field testing requires test power to be as low as worst-case functional power.

A Methodology for Creating Application Specific Processor Architectures

Prof. Anshul Kumar, IIT Delhi

Abstract

Performance improvement through datapath extensions with Application Specific Functional Units has been a subject of research for more than a decade now. However, we feel that full potential of this approach has not been exploited due to several obstacles. This talk presents techniques to get past some of these obstacles.

Usually a cluster of operations identified from the application defines a new custom instruction and forms the behavior of an Application Specific Functional Unit that implements this instruction. In the techniques available for identifying such clusters, the number of register file ports constrains the number of inputs and outputs for a legal operation cluster, thus limiting the overall achievable speedup. We present a technique that
circumvents the constraints imposed by register file ports and results in a significantly higher speed up. In addition, our identification algorithm runs 2 to 3 orders faster than a typical I/O constrained identification approach.

The second issue we take up here is estimation of the speedup achievable for the clusters identified. In order to select the right clusters, we need to correctly estimate the speedup taking into account what we call as temporal and spatial reuse of the clusters. In absence of efficient techniques to do so, researchers compromise either on the quality of estimates or on the number of clusters examined. We propose a novel method by which each cluster's reuse information can be derived very efficiently, making it possible to generate high quality custom instructions.

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VLSI Education: Beyond Digital and Beyond Moore's Law

Dr. Chandra Shekhar [1], Director CEERI

Abstract

Traditional VLSI educational curriculum for ME/MTech degree introduced in the late 1980s / early 1990s have served well the Indian VLSI industrial/services growth so far. However, several major new trends are emerging or becoming perceptible that require realignment of priorities and augmentation of syllabi, project/thesis directions and research directions.

The first trend is that analog design, mixed-signal design and RF IC design have now become very important areas that are occupying a significant part of the VLSI design space. These topics need to be addressed in the curriculum.

Issues of signal integrity, leakage currents and low-power design methods need to move into mainstream of the curriculum. Also, technologies and devices for pushing the limit of CMOS technology and Moore's law e.g. FinFETs, Multi-gate transistors, strained silicon, Si-Ge, etc. need to researched and the students should be made aware of these alternatives as well.

The second trend is reflected in the slowing down of Moore's Law and the challenge of delivering increasing performance even in the face of no further miniaturization. This needs to be addressed through architectural research --- with the right mix of application specificity in the hardware micro-architecture and the programming levels including new paradigms of programming.

The third trend is the search of new devices that can replace/supplement the MOS transistor as the vehicle of integration. The new devices on the horizon include resonant-tunneling devices (RTDs), single-electron transistor (SET), spin transistor, carbon nanotubes (CNT) based devices, molecular switch, graphene transistors, quantum electronics, etc. These need to be reasearched and their coverage needs to be brought into the curriculum.

A fourth trend is represented by the use of silicon for integration of micro-mechanical devices, micro-electromechanical devices, micro-sensors and micro-actuators. These components integrated alongside electronic circuitry for signal conditioning and processing can be used for building smart systems.

Additionally, areas like 3-D integration, formalisms and methodologies at electronic system level (ESL) design and SoCs need to be researched and taught.

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Design of Low Power & Robust Networks on Chip through Novel Coding Schemes

Prof. Partha Pratim Pande

Abstract

Our central vision is: Develop enabling technologies and tools spanning multiple abstraction levels to design globally optimized robust systems without incurring the high cost of traditional redundancy.

Design technologies for silicon-based integrated systems present unprecedented advantages and challenges, the former being related to the very high device density and the latter to the signal integrity issues. According to the International Technology Roadmap for Semiconductors (ITRS) with a chip area of about 500mm^2, in 50nm CMOS, over a thousand microprocessor cores, or modules of comparable complexity, may be integrated on to a single chip. The current design methodologies are not expected to provide the necessary design productivity to cope with the design of such big systems on chip (SoCs). Network on chip (NoC) is emerging as a revolutionary methodology to support this huge degree of integration. A major challenge that NoC design is expected to face is related to the intrinsic unreliability of the communication infrastructure under technology limitations. As the separation between the wires is reducing rapidly, any signal transition in a wire affects more than one neighbor. This phenomenon is commonly referred to as the crosstalk effect. Crosstalk is one of the sources of transient errors. Among other transient noise sources we can enumerate factors like electromagnetic interference, alpha particle hits, cosmic radiation, etc. To protect the NoC architectures against all these varied sources of noise it is possible to embed self-correcting design methodology and its corresponding circuit implementation in the NoC communication fabrics. This embedded intelligence can be achieved through simple and novel joint crosstalk avoidance and multiple error correction coding schemes. By incorporating these coding schemes we not only make the communication fabric robust, but also reduce the overall energy dissipation of the system.

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The Next Step in the SoC Design Automation

Manikandan Panchapakesan [1] and Ramachandra Vibhute [2]

Abstract

Nx-Builder is the standard NXP design environment that addresses the SoC (System on Chip) design challenges through extensive utilization of architecture, IP ReUse, efficient system integration, hardware-software (HW-SW) co-verification and design flow automation. Based on industry standards for design integration and advanced commercial design technologies, Nx-Builder helps in correct-by-construction designs and allows rapid development of new systems and platform derivatives. This tutorial introduces Nx-Builder to a broader audience and shows how it can be used to define, develop and verify a platform instance. This tutorial also highlights the features of Nx-Builder and illustrates how these differentiating design capabilities are being applied today to accelerate SoC development with silicon-proven results. Furthermore, the paper covers how Nx-Builder can be customized to cater for a wide range of platform architectures.

1. Introduction

Development methodologies for complex System-on-Chips (SoC) require increased levels of abstractions for IP handling. The overall platform and derived product development process will include specific and well-defined development responsibilities:

- IP creation
- IP level verification
- IP delivery, support and maintenance
- IP configuration, integration and system level verification

These development phases need to be supported by an automated and integral tool chain and technology. Nx-Builder targets definition and implementation of such a development methodology for platforms. Therefore its focus is on IP configuration and integration and most importantly system level verification.

Nx-Builder exploits the fact that most platform designs differ by relatively small amounts from each other and follow a small number of standard templates e.g.:

- Some peripheral blocks changes
- Some block parameters changes
- Bus structure changes

Majority of these changes can be automatically deduced from some basic design information, this means that the designer only needs to enter information on how their particular design differs from a reference design, they do not need to define the design from scratch and this information can then be used to drive the rest of the design process automatically. Nx-Builder exploits this methodology to allow

Robust System Design in Scaled CMOS and Emerging Nanotechnologies

Prof. Subhasish Mitra

Abstract

Our central vision is: Develop enabling technologies and tools spanning multiple abstraction levels to design globally optimized robust systems without incurring the high cost of traditional redundancy.

Specific ideas that will be discussed include:

1. Built-In-Soft-Error Resilience: An architecture-aware circuit design technique corrects radiation-induced soft errors in latches, flip-flops, and combinational logic at extremely low-cost compared to redundancy techniques;

2. Circuit failure prediction and self-correction: A new design technique, distinct from error detection, predicts failures before they actually create errors in system data and states. Circuit failure prediction is ideal for reliability mechanisms such as transistor aging and early-life failures, and can enable close to best-case design by minimizing traditional worst-case speed guardbands;

3. Imperfection-immune Carbon Nanotube Circuit Design: Misaligned Carbon Nanotubes (CNTs) pose a fundamental barrier to circuit design using Carbon Nanotube Field-Effect Transistors (CNFETs). An automated technique for designing imperfection-immune CNFET logic circuits guarantees correct implementations even in the presence of a large number of misaligned CNTs.

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Challenges posed to the state of the art device simulators in nanoscale regime

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Abstract

As the CMOS technology is approaching towards nanoscale regime, many novel ultra thin body device architectures have been proposed to boost up its performance. However to evaluate the electrostatics and carrier dynamics of these nanoscale devices the state of the art device simulators which employ semi-classical model of carrier transport like Hydrodynamic(HD) transport model are not very accurate even though they consider some quantum corrections like Van Dort's model, density gradient model, modified local-density approximation (MLDA) model etc. So, it has become extremely important to move towards quantum mechanical approach based simulation techniques. One such approach is based on Non-Equilibrium Green's Function (NEGF) formalism. In this paper, we present the comparison between the simulation results obtained from professional device simulator (Sentaurus) and quantum mechanical simulators (NanoMOS, Nanowire) for multigate ultra thin body devices. The Hydrodynamic transport model, derived from Boltzmann's transport equation (BTE) is used for the semi-classical carrier transport analysis. The quantum transport analysis has been studied using the simulation tools, which are based upon NEGF formalism. The result of this work shows that quantum mechanical approach correctly describes both the electrostatics and the carrier transport of these mesoscopic devices.

Keywords: CMOS Scaling, Ultra thin body device, Hydrodynamic Transport, Boltzmann's transport equation, Non-Equilibrium Green's Function

1. Introduction

Computer Aided Design and accurate simulation tools of electron devices has been one of the major factors contributing to the success of the semiconductor industry. At the same time to continue the scaling trend for the next few decades many novel ultra thin body device architecture have been emerged in the last few years. Regardless of what form future electronic devices take, we will have to learn how to model and describe the electronic properties of device structures that are engineered in nanoscale. Because in this nanoscale regime devices exhibit many quantum effects like volumetric inversion, source to drain tunneling, coulomb blockade which are not properly captured by semi-classical model. The reason for this is most of the carrier transport models used in

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