A Novel Distributed and Interleaved FIFO for Source-Synchronous Interconnect

Santosh Sood [1], Mark Greenstreet[2], Resve Saleh[3]

Abstract

In deep submicron technologies, various techniques of interconnect pipelining are used, where long buses are broken in to short segments by inserting the buffers and latches or flip-flops. The synchronous pipeline has overheads due to the clock distribution network, whereas the asynchronous techniques are limited by round-trip delay of the wire. Source-synchronous methods of interconnect pipelining entail forwarding the clock along with the data. The forwarded clock suffers from skew due to process, voltage and temperature (PVT) variations along the forwarded path. Source-synchronous signaling further suffers from the additional latency of skew compensating FIFO at the receiver. In this paper, we present a novel, distributed and interleaved FIFO that hides the control latency by enabling wave pipelining between the FIFO stages. We introduce a metric of comparison called velocity, and compare the performance of source-synchronous link with the time borrowing two-phase and flip-flop based synchronous design. The two-phase time borrowing scheme achieves best performance. The distributed and interleaved approach outperforms the flip-flop based synchronous communication over wide range of throughput and velocity targets as well as not requiring global clock distribution. These qualities make our design well-suited for solving SoC interconnect challenges.

Keywords: *interconnect pipelining, source-synchronous, FIFO, velocity metric.*

1. Introduction

In high-performance designs, the time to transmit a signal across a long interconnect can be several clock periods, and the gap between logic and interconnect performance will continue to widen in future processes [Ho,99]. One way to address this problem is to implement interconnect pipelining, where we introduce buffers and latches in the long interconnect. The total path delay for a signal to cross in a clock cycle is effectively reduced to that of the delay of buffers and wires between two memory elements.

In this paper, we compare two approaches for interconnect pipelining: register pipelining and source-synchronous communication. We examine the common case where a single clock is distributed to the entire chip and the registers are either transparent latches that can be enabled on either polarity of the clock or edge-triggered flip-flops. We then consider an idealized scenario where any desired clock phase is available at any point in the chip. It provides an upper bound on the performance that can be achieved by various techniques of interconnect pipelining. In a source synchronous design, the sender forwards a

[1]Texas Instruments, India. santoshs@ti.com
[2]University of British Columbia, Canada. mrg@cs.ubc.ca
[3]University of British Columbia, Canada. res@ece.ubc.ca

HANDLING TRAPEZOIDAL CONDUCTOR CROSS-SECTIONS IN A STATISTICAL CAPACITANCE EXTRACTOR

Subramanian Rajagopalan, Shabbir Batterywala[1]

Abstract

Interconnect cross-sections are increasingly trapezoidal in nature due to under-etching and electrolytic growth. With the reducing spacing between interconnects and interconnects themselves becoming narrower and longer, the effect of trapezoidal shapes on parasitics can no longer be neglected. In this work, a statistical capacitance extractor was modified to handle trapezoidal conductor cross-sections. It was then used to study the effect of trapezoidal cross-sections on interconnect parasitic capacitances. The results are compared to those obtained by approximating trapezoids as a set of stacked cuboids varying in size like a staircase.

1. Introduction

With the advent of deep sub-micron technologies, on-chip interconnects have become significantly narrower and closer. In addition, the cross-section of interconnects are not rectangular. Due to manufacturing phases like etching and electrolytic processes, the cross-section of interconnects are closer to trapezoids than cuboids [Dengi and Roher (1997)], [Saute, Rein, Frerichs, Landsiedel, Thewes and Weber (2000)]. Given the need for accurate parasitics extraction to perform signal integrity analysis and obtain timing closure, it is imperative to consider variations in interconnect cross-sections during the extraction process. Deepak *et. al* show that the presence of trapezoidal cross-sections in off-chip interconnects is an important problem in parasitic capacitance extraction [Nayak, Hwang, and Turlik (1989)]. They show that coupling capacitances can vary as much as 30% and self capacitance can vary by 12% in the presence of interconnects with trapezoidal cross-sections. Conductor cross-sections, particularly trapezoidal cross-sections, have been recognized as an important problem in the area of CAD [Zhu and Yamashita (1995)], [Zhu, Pun, and Chung (1996)].

One of the most common techniques to compute capacitance (C) is to compute the charge (Q) for a given voltage (V) and then use the relationship between Q and V, Q=CV, to obtain C. Computing Q in-turn involves evaluating a charge integral. Several techniques have been proposed to compute this charge integral involved in capacitance extraction. Boundary Element Method (BEM) based solutions solve charge equations arising out of discretization of conductor

[1] Advanced Technology Group, Synopsys India Private Limited

Implementation of MPEG4 Video Decoder on a SoC Multimedia Processor

Prashanth P [1], Raghuveer P S [2], Vinayak A.S [3], and C.R.Venugopal [4]
[1] prashanth.p@celstream.com, [2] raghuveer.ps@celstream.com, Celstream Technologies
[3] SJCE, Mysore asvinayak@yahoo.com, [4] Prof. SJCE, Mysore
cr_venu@yahoo.com

Abstract: MPEG-4 [1] is the newly defined standard from the Moving Pictures Experts Group (MPEG). There are different profiles and levels supported in the standard [2]. This paper briefs the work carried out as part of the M.Tech Project at Celstream Technologies, Bangalore. The implementation of MPEG4 Advanced Simple Profile (ASP) is done on a System on Chip (SoC) Multimedia Processor. The decoder is capable on decoding the elementary MPEG4 Video bitstream which is stored in the external DDRAM of the Multimedia processor system. This bitstream is stored in the DDRAM through streaming. The video bitstream is decoded to be displayed at 25 to 30 frames per second (fps). The software developed for this processor involves both C and assembly.

Keywords: MPEG4, SoC, Advanced Simple Profile, SIMD, RISC, LEON.

I. INTRODUCTION

MPEG-4 is an ISO/IEC standard with designation ISO/IEC 14496[1]. MPEG-4 standard improves on MPEG-2 standard in both compression efficiency and coding flexibility, and hence covers a wider range of applications. MPEG-4 part 2 (visual coding) standard was developed to address applications in emerging fields in areas such as digital television, interactive graphics with synthetic contents, interactive multimedia over the internet, and interactive video games. MPEG4 provides a common technical solution to various communication paradigms - telecommunications, broadcast and interactivity. While MPEG-4 itself comprises a toolbox of coding instruments, the combination of specific coding tools is organized in profiles and levels, each targeting a preferred application field [2]. As more important multimedia applications continue to emerge, new profiles are under consideration. Several new tools were added to achieve this superior coding efficiency: B-VOPs and advanced motion compensation tools such as quarter-pel (QMC) and global motion compensation (GMC), as well as sophisticated post-processing [4] tools for deblocking and deringing. However, all these tools add significantly to the complexity of the overall decoding process. The SoC [5] used as a platform is a Thomson proprietary architecture which consists of three SPARC RISC cores known more popularly as LEONs. These RISC processors serve to control the main pixel crunching processors and also carry out some bitstream parsing and synchronizations issues.

The use of SIMD architectures for achieving this parallelization or vectorization [7] of the IDCT and the Motion compensation tasks is all but necessary. Since the decoding process involves a lot of memory referencing activity, and also the memory is accessed in large chunks. It is necessary that there exists an effective memory bandwidth [8] utilization strategies.

HIGHLY LINEAR & HIGHLY EFFICIENT POWER AMPLIFIER DESIGN USING DIODE NONLINEAR CAPACITANCE

Mrunal. A. K[1], Makarand Shirasgaonkar[2], Rajendra Patrikar[3]

Abstract

The emphasis on higher data rates and spectral efficiency has driven the industry towards linear modulation techniques such as QPSK, 64 QAM and other multi-carrier configurations. These modulated signal have a fluctuating envelope (higher peak to average ratio). When amplified by non-linear power amplifiers they cause spectral regrowth as well as intermodulation distortion (IMD) in power amplifiers.

This paper describes a novel approach of using a diode as an active linearizer for minimizing non linear distortion introduced by the power amplifiers in wireless communication circuits. This approach is based on preventing the base-collector junction from becoming forward biased in the case of HBTs, there by keeping it in active region. It compensates the nonlinear input capacitance of HBTs and BJTs. In case of pHEMTs and MOSFETs this technique reduces the effect of nonlinear terms generated by the voltage variable input capacitance of the active device.

A two stage power amplifier designed using 0.5µm GaAs pHEMT process shows that the power amplifier is linear up to 10dBm of input power after linearization, where as it becomes nonlinear at -4dBm of input power before linearization at 2.45 GHz. HBT power amplifier shows 2 dBm improvement in the output power while MOSFET power amplifier shows 4 dBm improvement in the output power. This MOSFE power amplifier becomes nonlinear at 13 dBm of input power whereas it is linear up to 17 dBm of input power after linearization.

Keywords*: Power Amplifier, Intermodulation Distortion, Linearization*

1. Introduction

Linear/pseudo linear power amplifier design techniques are required in wireless communication circuits that employ multi-carrier modulation techniques. Various techniques have been proposed for power amplifier linearization. The digital predistortion technique [1] [2], offers good

[1] Research Associate, Nanoelectronics Centre, Department of Electrical Engineering, Indian Institute of Technology - Powai & affiliated to VLSI design lab, VNIT, Nagpur. Email: mrunalak@gmail.com

[2] Member of Technical Staff , Qualcore Logic Ltd. , Hyderabad & affiliated to VLSI design lab, VNIT, Nagpur . smakarand@yahoo.co.in

[3] Professor, Department of Electronics, Visvesvaraya National Institute of Technology (VNIT), Nagpur, India. rajendra@computer.org

Novel Architecture of Context Modeling for JPEG2000 and a Comparison with Taubman's Architecture

K. Pratyush Aditya[1]
Anand Gautam[2]
A. Geeta Madhuri[3]
Priya Khandelwal[4]
DA-IICT, Gandhinagar, Gujrat

Abstract

Context Modeling block of JPEG2000 is one of the most computation intensive process. Taubman's architecture is a standard architecture used for the process. The paper draws a comparison between the standard Taubman's Architecture and the proposed architecture. The paper depicts how the drawbacks of Taubman's Architecture: 1) Sequential bit-plane processing and 2) Large memory interactions can be removed. The proposed architecture presents two speed-up methods: 1) n bit-plane parallelization and 2) Three stage pipelined architecture of Context calculation blocks. Consequently the design would enhance the throughput and reduce latency with respect to other standard architectures present. The synthesis and implementation of the design was done on 0.13µm and 90nm technologies using Cadence RTL Compiler.

1. Introduction

JPEG2000 scores over its predecessor JPEG in terms of:

- Better image quality at all compression ratios
- Error resilience in noisy environments
- Superior lossless and lossy compression in a single code stream
- Singular compression architecture

It also supports various new provisions that were not present in its predecessor:

- ROI (region of interest) coding.
- Large image handling i.e. images as big as *64k* x *64k* can be compressed at a time without tiling.
- Better performance on computer generated pictures and text documents etc.

All these enhancements and improvements over JPEG come with a liability of high computation intensive operations.

[1] pratyush.aditya@gmail.com
[2] gautamanand4@gmail.com
[3] geeta.madhuri@gmail.com
[4] priya219@gmail.com

AUTOMATIC TEST GENERATION FOR TEMPORAL COVERAGE POINTS USING A STOCHASTIC TREE MODEL

Anindyasundar Nandi*, Bhaskar Pal*, Pallab Dasgupta*, Partha P. Chakrabarti*

Abstract

In recent times, the industry is moving towards a coverage driven randomized test generation approach, as opposed to the traditional practice of writing directed tests. This methodology does not require manual effort in writing directed tests and thereby validation reaches a larger coverage in less time. The main drawback of an unconstrained random approach is that several corner case scenarios that involve complex input patterns are not covered easily because of the low probability of occurrence of such scenarios. This has prompted proponents of the new approach to constrain the test generation so that coverage points can be visited early. This paper proposes a methodology for specifying temporal constraints and using them during adaptive test generation. The results show the effectiveness of the approach. The tool flow can easily be incorporated in the current validation flow.

Keywords: Test Generation, Coverage, Stochastic Methods.

1. Introduction

It is widely accepted that validation accounts for more than 70% of the design cycle time. A significant fraction of this time is spent on identifying coverage points and writing directed tests to cover the desired scenarios. The steep rise in the complexity and the number of directed tests that are required to achieve meaningful levels of coverage has prompted the industry to move towards a coverage driven randomized test generation (CDG) approach [2] [8].

The key idea of CDG-based verification is simple. An automatic test generator generates random tests. Coverage monitors are used to determine whether user defined coverage goals are reached. Typically each coverage goal consists of a property and a number which indicates the number of times the user would like to visit a state where the property holds. Recent verification methodologies that use CDG-based verification include VMM (ARM & Synopsys) [11], RVM

* Department of Computer Sc. & Engg, IIT Kharagpur - 721302
{anindya,bhaskar,pallab,ppchak}@cse.iitkgp.ernet.in

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EFFICIENT DRC FOR VERIFICATION OF LARGE VLSI LAYOUTS[1]

P.K. Ganesh[2] **Prosenjit Gupta[3]**

Abstract

The traditional mask-based model employed for Design Rule Checking (DRC) results in problems amenable to easy solutions by standard techniques in Computational Geometry. However, when dealing with data sets too massive to fit into main memory, communication between the fast internal and the slow external memory is often the chief performance bottleneck. Although a lot of research has been done in the recent past on efficient external-memory algorithms and data structures, such work in the area of VLSI computer-aided design is limited. In this paper, we design efficient external memory algorithms for a number of prototypical problems in DRC by exploiting the so-called square root law, which states that in a VLSI layout set of n line segments, we can expect about $\sqrt{n}$ segments to intersect a horizontal or vertical scanline. These algorithms are found to substantially outperform existing main memory algorithms as well as worst-case optimal external memory algorithms which ignore the square root law.

Keywords

External Memory Algorithms, Design Rule Checking, VLSI Layouts

1. Introduction

In an increasing number of problems these days, including those involving VLSI layouts, the amount of data to be processed is often far too massive to fit into internal memory. Despite growing memories, the increasing demands on tools to handle larger amount of data necessitates taking secondary management into account explicitly. One can certainly use standard main memory algorithms for data that reside on disk but their performance is often considerably below the optimum because there is no control over how the operating system performs disk accesses. Algorithms and data structures designed to minimize the I/O operations between main memory and disk are called *external-memory algorithms* (Vitter (2001)). Although a lot of research has been done in the recent past on efficient external-memory algorithms and data structures in general, such work in the area of VLSI computer-aided design is limited. In Liao, Shenoy and Nicholls (2002), an efficient external-memory algorithm for the region query in area routing was presented. In Sharathkumar, Vinaykumar, Maheshwari and Gupta (2005), an efficient external-memory segment-intersection algorithm was presented, assuming that the data originates from VLSI layouts.

[1] Research supported by DST grant SR/S3/EECE/22/2004.
[2] I.I.I.T. Hyderabad. Email: ganesh@students.iiit.ac.in.
[3] I.I.I.T. Hyderabad. Email: pgupta@iiit.ac.in.

RF ENERGY SCAVENGING FOR WIRELESS SENSOR NODES

Shantanu Bhalerao[1], Abhishek Chaudhary[2], Raghavendra Deshmukh[3], Rajendra Patrikar[4]

Abstract

The modern VLSI techniques have reduced the power consumption of low power electronic systems to tens of microwatts. This creates an opportunity to power these systems using ambient energy from the environment. In this paper, we propose a method to power wireless sensor nodes by converting ambient RF energy in the 2.4 GHz ISM band into DC power. In general, this method can be applied to supply power to low power VLSI systems in an office space. Our system consists of an antenna array, a diode detector circuit and DC power management module. We discuss the design of a diode detector circuit using zero biased Schottky diode and the output DC voltage for different incident RF power levels. A folded patch antenna with dimensions 7.5 mm x 7.5 mm x 5.5 mm is designed.

1. Introduction

Advances in low power VLSI have pushed down the power requirements of low power micro systems to tens of microwatts [1][2]. This opens up many possibilities of powering these micro systems using ambient energy from the environment. Energy scavenging or recycling ambient energy leads to systems that have longer lifetimes and reduces maintenance costs. In this method, we present the method of powering sensor nodes using ambient RF power and this method may be applied to other low power systems as well.

Wireless sensor networks can be put to use in numerous scenarios such as construction industry, medical monitoring, intelligent office spaces, automatic manufacture units, and military applications. They are likely to be dense networks scalable up to thousands of nodes that collect information and valuable inferences may be drawn from the information collected over a period of time. It is possible to operate sensor nodes with power in the range of hundreds of microwatts by keeping the duty cycle of the sensor node low. In this paper, we present a system that avoids fixed energy sources such as batteries and employs ambient RF energy to power the sensor nodes.

[1] sbhalerao@gmail.com
[2] abhishek.vnit@gmail.com
[3] rbdeshmukh@vnitnagpur.ac.in
[4] rajendra@computer.org

A DEDICATED PROCESSOR TO REALIZE INVERSE RADON TRANSFORM FOR CT IMAGING

Abhishek Mitra[1], **Swapna Banerjee**

Abstract

The recent modification to an existing reconstruction algorithm (Inverse Fast Radon Transform or IFRT) of Computed Tomography (CT) significantly reduces the computational complexity and flow path complexity of this algorithm, thereby making its VLSI implementation feasible. An FPGA based dedicated hardware processor is presented here to implement Modified IFRT. Affordable parallelism has been incorporated into the hardware system to speed up the computation for CT images. Also, on-line generation of some fixed coefficients eliminates the need of huge memory requirement. The maximum speed of operation is found to be 103.98 MHz.

Keywords: *Inverse Radon transform, tomographic image reconstruction, FPGA, dedicated processor, parallel processing, memory efficiency.*

1. Introduction

Inverse Radon transform is the mathematical basis of CT image reconstruction from the collected X-ray data of the patient e.g Kak and Slaney [1988]. As data collection capabilities and image reconstruction algorithms have become more sophisticated the computational intensity of CT imaging has drastically increased and a dedicated hardware processor designed specifically for a particular reconstruction algorithm appears to be the only solution to this problem e.g Hurst et al. [1990], Shieh et al. [1992], Coric et al.[2002].
The "Fast Radon Transform" (FRT) and its modification are given in Kelly and Madisetti [1993] and Mitra and Banerjee [2004] respectively, which shows a very regular algorithm and all its steps viz. FFT/IFFT, Vector-Matrix multiplication are very suitable for VLSI implementation. Here we present an FPGA implementation of the IFRT algorithm targeting a fast CT image reconstruction system. Our hardware architecture is based upon a theoretical framework to meet all the criteria's viz. parallelism, memory minimization etc. for an efficient hardware system.

2. Fast Radon Transform (IFRT) and Inverse Fast Radon Transform (IFRT).

The Modified FRT uses the simplest flow path of the FRT algorithm. Therefore, a flow diagram of IFRT is given in Fig.1, where we have assumed that forward

[1] Contact Information: Abhishek Mitra, IIT Kharagpur. mitra_avi@yahoo.co.uk

HIGH PERFORMANCE AND AREA EFFICIENT n-BIT TREE BASED BINARY SQUARER

Gopal Paul[1], Research Scholar **Samir Satpathy**[1], Student

Abstract

Binary squarer is one of the frequently-used devices required in several applications like image processing, vector quantization etc. Traditionally, the techniques for multiplying two numbers are, Wallace Tree multiplier, Array multiplier etc. Wallace Tree multiplier is considered to be the most organized multiplier but, can be optimized in area and performance by removing redundancy in multiplying two numbers, which are the same. The proposed n-bit binary squarer overcomes these problems efficiently. For a 32-bit squarer, nearly 52% reduction in full adders and over 45% reduction in total number of gates have been found.

1 Introduction

In many VLSI applications, like digital signal processing, image processing, vector quantization etc, the computation of the square of a binary integer number is extensively required. This squaring operation can generally be implemented using multipliers like Wallace Tree Multiplier (WTM) by Wallace (1964), Array multiplier and several other techniques proposed by Fadavi-Ardekani (1993), Ienne and Viredaz (1994) and Wang, Jullien and Miller (1995). Wallace Tree multiplier is most commonly used because of its symmetric performance and minimum propagation delay. It uses carry-save adders to add 3-bits at a time. But when the multiplier and multiplicand are the same, the redundancy in partial products can be eliminated to save a lot of area and delay in the circuit. We, in this paper, have mainly focused on the removal of unnecessary redundant operations leads to much lesser number of full-adder operations to make the device faster and area efficient.

In the next section we have explained our technique with the example of 8-bit binary squarer. The whole multiplication is divided into three steps. WTM starts the addition operation at step1 whereas our technique approaches towards step2 and step3 for generating the optimized partial products. Section 3 highlights our algorithm with the necessary pseudo-code and section 4 shows the comparison results after running our algorithm for n-bit squarer. Section 5 concludes briefly mentioning the usefulness of our technique.

[1] Dept. of Computer Science & Engg., IIT-Kharagpur, WB, India

ENERGY EFFICIENT APPLICATION SPECIFIC BANKED REGISTER FILES

Rakesh Nalluri[1] **Preeti Ranjan Panda**[1]

Abstract

Register files account for a significant fraction of the power dissipation in modern RISC processors. Register file banking is an effective alternative to monolithic register files in embedded systems. We propose a profile-based technique to arrive at a customized energy-efficient bank configuration for a given application on a dual bank register file. The technique consists of a register renaming step take advantage of the bank structure of the register file by renaming the most frequently accessed registers to the smaller bank. Experimental results indicate that our approach gives energy savings of 40-50% on register files with customized bank configuration.

1. Introduction

Low power design is becoming an integral part of embedded system design with the profusion of mobile devices. Increasing computation requirements for audio/video applications in portable devices implies the need for long life battery devices and reduced energy dissipation. As battery improvement techniques are not able to satisfactorily address the growing energy requirements of processors, it is important to devise new low power architectural techniques to reduce microprocessor power consumption.

Register files account for a significant fraction of the power budget of typical RISC processors. Even in RISC processors designed for low power applications like Motorola's M-CORE processor (Scott et al. (1998)), register file consumes about 16% of total processor energy consumption and 42% of total data path energy consumption. Partitioned register files are interesting options for RISC processors, as monolithic register files are becoming bottlenecks for power and performance. Register file partitioning reduces the overall switching, thereby reducing energy consumption in the register file. Several studies have shown the effect of register file partitioning on power and performance in embedded and superscalar processors ((Cruz et al. (2000); Balasubromonian et al. (2001); Zyuban and Kogge (1998)).

Register file access in RISC processors is highly asymmetric in nature; a relatively small number of registers account for a majority of the register file accesses during program execution. This is mostly because the lifetime of typical program variables is very small and a small number of registers are heavily reused. Also, because of calling conventions followed in most RISC processors; these are rules enforced by the software during procedure call on

[1] Department of Computer Science & Engineering, IIT Delhi, India

Detecting Faults at the Time They Occur

Abhijeet Kumar Sayantan Das Pallab Dasgupta, P. P. Chakrabarti[1]

Abstract

With the gaining popularity of dynamic Assertion based verification among the validation engineers one of the major requirement that comes to the forefront is to develop efficient and simple methodologies to interpret the results of assertions during simulation. This is important for detecting and correcting design errors. One major problem with some properties is that the cause of its failure and time of its violation during simulation might take place at different times. Such properties are called unreceptive properties. This feature of the unreceptive properties causes detection of design errors difficult. In this work we propose a methodology and algorithms to automatically convert an unreceptive specification to a receptive one by adding (there by enriching) more properties to the specification. We have also developed a tool called toReceptive and tested it over some industry standard verification IPs.

Keywords: *Formal Specification, Verification*

1. Introduction

Assertion-Based Verification (ABV) is assuming a significant role in the design validation flow of chip design companies. In recent times active participation from the design and EDA industries have led to the adoption of several formal languages for assertion specification. These include Sugar/PSL (of IBM/ Accelera) [15] and OVA (of Synopsys) [10]. Several companies are developing / marketing dynamic ABV verification IPs for standard protocols, such as PCI Bus [11], ARM AMBA Bus [2], and Hypertransport [6].

In dynamic ABV, we verify whether the design conforms to its assertions during simulation. The failure of an assertion reflects the presence of a design error and the validation engineer needs to examine the source of the error that leads to the failure of the assertion. Recent experience shows that this is a non-trivial task since the assertions are temporal in nature and as a result, an assertion failure may occur several cycles after the occurrence of a fault. It is possible to write specifications in a way such that each fault is covered exactly on the cycle in which it occurs, but it is not practical because the number of properties would be vast.

In many cases, the failure of an assertion becomes imminent when the existing dynamic ABV checkers do not detect this fast. Rather, the matching of the

Contact Information: Department of Computer Science and Engineering,
Indian Institute of Technology, Kharagpur India. Pin 7213102.
Email: abhij_kr1@yahoo.com, {sayantan,pallab,ppchak}@cse.iitkgp.ernet.in

CONSTRUCTING ONLINE TESTABLE CIRCUITS USING REVERSIBLE LOGIC

Sk Noor Mahammad, Siva Kumar Sastry Hari, Shyam Shroff and V Kamakoti[1]

Abstract

Testable fault tolerant system design has become vital for many safety critical applications. On the other hand, reversible logic is gaining interest in the recent past due to its less heat dissipating characteristics. Any Boolean logic function can be implemented using reversible gates. This paper proposes a technique to convert any reversible logic gate to a testable gate that is also reversible. The resultant reversible testable gate can detect online any single bit errors that include Single Stuck Faults and Single Event Upsets S.Karp et.al (1993). The proposed technique is illustrated using an example that converts a reversible decoder circuit to an online testable reversible decoder circuit.

Keywords: *Reversible Logic, Online Testing, Power Dissipation, Digital Circuits.*

1. INTRODUCTION

Reversible Logic has gained importance in the recent past. The rapid decrease in the size of the chips has lead to the exponential increase in the transistor count per unit area. As a result, the energy dissipation is becoming a major barrier in the evolving nano-computing era. Reversible logic ensures low energy dissipation R.W. Keyes et.al (1970), C.H. Bennet (1988). An operation is said to be physically reversible if there is no energy to heat conversion and no change in entropy. In reversible logic, the state of the computational device just prior to an operation is uniquely determined by its state just after the operation. In other words, no information about the computational state can ever be lost and hence the reversible logic can be viewed as a deterministic state machine. R.Landauer (1961) has shown that for every bit of information that is erased during an irreversible logic computation kTln2 joules of heat energy is generated, where k is the Boltzmann constant and T is the temperature in Kelvin at which the system is operating. C.H.Bennett (1973) showed that the kTln2 amount of energy dissipation would not occur if a computation is carried out in a reversible way.

Computations performed by the current computers are commonly irreversible, even though the physical devices that execute them are fundamentally reversible. At the basic level, however, matter is governed by classical mechanics and quantum mechanics, which are reversible. With computational device technology rapidly approaching the elementary particle level, it has been argued many times that this effect gains in significance to the extent that efficient operation of future computers requires them to be reversible

[1] Reconfigurable and Intelligent Systems Engineering Group, Dept. of Computer Science & Engg. IIT Madras, Chennai.

Detection of Bridging Faults in Reversible Circuits

Hafizur Rahaman[1], *Dipak K. Kole*[1], *Debesh K. Das*[2]
Bhargab B. Bhattacharya[3]

[1]IT Dept., Bengal Engg. & Science University, Howrah – 711 103, India
[2]CSE Dept., Jadavpur University, Kolkata – 700 032, India
[3]ACM Unit, Indian Statistical Institute, Kolkata – 700 108, India
Email: [1]*rahaman_h@yahoo.co.in* , [2]*debeshd@hotmail.com*, [3]*bhargab@isical.ac.in*

Abstract

Test generation under the bridging fault model in a reversible circuit is studied in this paper. Only intra-level bridging faults are considered to be present, i.e., a single pair of lines, both lying at the same level of the circuit, may be assumed to have been logically shorted for modeling a defect. For a reversible circuit realized with simple Toffoli gates, an $O(Nd^2 \log_2 N)$ procedure is described to generate a complete test set that detects all such single intra-level bridging faults, where N and d represent the number of inputs and depth of the circuit respectively. A test set of cardinality $O(d \log_2 N)$ will be sufficient for this purpose.

1. Introduction

Reversible logic can be employed to design information lossless circuits [1-3]. An *n*-input, *m*-output Boolean function *F* is said to be reversible if and only if $m = n$, and *F* is one-to-one. A combinational logic circuit is said to be reversible if it is fanout free, acyclic, and consists of only reversible gates, which themselves implement reversible functions; such gates need to be specially designed, e.g., Toffoli gates. Reversible circuits have manifold applications to optical computing, digital signal processing, communication, cryptography, nanotechnology, quantum computing, DNA technology, and low-power CMOS design [5-13]. If IC technology continues to follow the pattern predicted by the Moore's Law [4], energy loss in non-reversible design is likely to become more dominant, and reversible logic may offer a viable solution in the future with newer technologies.

Conventional logic gates such as AND, OR, or EXOR used in digital design are not reversible. Only the NOT gate is reversible. To design a reversible circuit, only reversible gates can be used, for example, the *controlled-not* (CNOT) gate proposed by Feynman [14], Toffoli [16], and Fredkin [15] gates. Several techniques for synthesis of reversible logic circuits are available [17-23].

The problems of fault modeling and testing of reversible logic circuits have been studied recently by several researchers [24, 27-30]. Reversibility was studied in the context of on-line testing of irreversible circuits [25, 26]. Patel et al. [24] focused on testing of inherently reversible circuits, and addressed the test generation problem. It was observed that only a few test vectors are necessary to fully test a reversible circuit under the multiple stuck-at fault model; the test size grows at most logarithmically both in the number of inputs and in the number of gates. Thus, reversible circuits seem to be much easier to test than their

SOC IMPLEMENTATION OF THE NEURAL NETWORK BASED ISOLATED WORD RECOGNITION

V. Amudha*, B.Venkataramani†, J.Karthick‡ and C. Praveen ‡

Abstract:

System on chip implemented using FPGAs can be configured to have both general-purpose microprocessors and custom blocks optimized for specific functions. This enables a system to be optimally partitioned into software and hardware. In this paper, the SOC based implementation of an isolated word recognition system using both SOFM and MLP neural network is considered. For the implementation, Altera UP3 kit with NIOS II soft-core processor is used. The feature extraction and training blocks are implemented in software. The speech recognition block is implemented on SOC in both software and hardware and is compared. The hardware implementation is found to be 21 times faster than the software implementation without degradation in recognition rate. One of the factors responsible for speed-up with the hardware approach is the implementation of the sigmoid activation function in hardware using RAM blocks. To minimize the area requirement, floating point operations are replaced by fixed-point operations. Two-stage pipelining is used for multiplications and additions. With these optimizations, an overall recognition percentage of 95 is achieved for an 18 by 18 feature map.

Key words: SOC, SOFM, MLP, LUT, pipelining, sigmoid function

1. Introduction:

In the literature, neural network has been applied successfully to many problems in the areas of pattern recognition, signal processing, time series analysis, etc. In particular, the application of neural networks to speech recognition has attracted considerable interest in the recent past. For isolated word recognition, the artificial neural network (ANN) is used for modeling the dynamic and static properties of speech signals within a word in [1]. Software simulations are useful for investigating the capabilities of neural network models and creating new algorithms, but hardware implementations remain essential for taking full advantage of the inherent parallelism of neural networks. Traditionally, ANNs have been implemented directly on special-purpose digital and analogue hardware. More recently, ANNs have been implemented with re-configurable FPGAs. Although FPGAs do not provide better performance than the custom chips in terms of power dissipation, clock rate, or gate density, they do provide a speed-up of several orders of magnitude compared to software simulation [2]. In view of this, the FPGA implementation of neural network based speech recognition system is considered in this paper.

- Research Scholar, Department of E.C.E, N.I.T, Tiruchirapalli, amudha@nitt.edu
- j Professor, Department of E.C.E, N.I.T, Tiruchirapalli, bvenki@nitt.edu
- k Student, Department of E.C.E, N.I.T, Tiruchirapalli

DESIGN OF HARDWARE COPROCESSOR FOR OTDR APPLICATION

S.Ponnmozhi, Nitin Chandrachoodan[1]

Abstract

The design and implementation of a hardware coprocessor for Optical Time Domain Reflectometry applications is described. OTDR applications require processing data sampled at high rates (upwards of 50MHz), and signal processing operations such as filtering and event detection need to be applied to the resulting signal traces. This usually requires some specialized hardware, and previous approaches have considered designs based on multiple chips to accomplish the task.

In this paper, we present a single chip implementation of the data acquisition and processing parts of the system on a Field Programmable gate array (FPGA). The design is modular, using coprocessor modules to interface with a main microprocessor core. This design approach allows easy extension of the system to add new types of functionality such as additional signal processing power.

Keywords : OTDR, FPGA, Coprocessor, MicroBlaze

1. Introduction

Optical Time Domain Reflectometer (OTDR) [1] is a test equipment to detect faults within an optical link. It measures parameters such as attenuation, length, connector and splice losses and reflectance levels. Optical links primarily made of glass suffer from structural inhomogeneities, manufacturing defects, compositional fluctuations and microscopic variation in the material density. These give rise to refractive index variations, which occur within the glass over distances that are small compared with the wavelength. This causes Rayleigh-type scattering of the light. Another phenomenon resulting in reflection of light is known as Fresnel reflection. This occurs at the fiber-core end face. As light propagates along the fiber, a fraction of the light gets scattered and reflected due to the phenomena described above. This backscattered light is captured by the instrument and analyzed to characterize the fiber. The locations of the faults are determined by injecting a pulse of light using a laser and measuring the strength of the returned light as a function of time.

The performance of an OTDR is specified by parameters such as dynamic range, measurement range, event dead zone and resolution [4]. The returned light obtained after injecting a light pulse into the fiber is degraded by addition of noise in the system. The signal-to-noise-ratio (SNR) can be improved for higher dynamic range by averaging several backscattered signals that are obtained as a result of injecting laser pulses into the fiber. The pulse width plays an important role in terms of resolution and dynamic range. A small pulse width

[1] Department of Electrical Engineering, IIT Madras.

AN ENERGY-EFFICIENT PACKET FILTERING ARCHITECTURE FOR WIRELESS SENSOR NODES

Prashant Sonone[1], Saswat Chakrabarti[2]

Abstract

The energy-efficient communication among wireless sensor nodes determines the lifetime of a sensor network. This paper presents an energy efficient packet filtering architecture and its implementation on FPGA. Our architecture takes into account the advantages of both the intelligence of the RF transceiver CC1000 and the need of applications to efficiently handle the packet dropping. The architectural design is discussed along with device utilization details. Our analysis shows 39% energy saving can be achieved with low hardware complexity.

Keywords
Wireless Sensor Networks, Packet Filtering and Forwarding

1. Introduction

In recent years, an exciting new type of networks has emerged called sensor networks [1]. Contrary to more traditional computer networks, these sensor networks consist of a large number of ultra-small autonomous devices. Each device, called a sensor node, is battery powered and equipped with integrated sensors, limited data processing capabilities, limited memory and short-range radio transceiver (ISM frequency band) [2]. A sensor network can be viewed as a distributed autonomous system for information gathering, thereby performing tasks such as terrain surveillance, wildlife monitoring, etc. In typical application scenarios, the nodes are spread out randomly over the terrain under scrutiny and collect sensor data [2]. The node processes this data and coordinates with nearby nodes to combine their information [1]. The aggregate data is then forwarded to specialized gateway nodes (base stations), connected to a computer for higher level of processing, which in turn provides remote access to the sensor network via Internet.

Sensor nodes are battery driven and hence operate on an extremely frugal energy budget [3]. Further, they must have a lifetime on the order of months to years, since battery replacement is not an option for networks comprising of very large

[1]Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology,Kharagpur. prashant@ece.iitkgp.ernet.in
[2]G.S.Sanyal School of Telecommunication, Indian Institute of Technology, Kharagpur. saswat@ece.iitkgp.ernet.in

A NOVEL ALL DIGITAL PHASE LOCKED LOOP FOR PHASE TRACKING IN GPS RECEIVERS

S Moorthi[1] K Pavithra[2] J Raja paul perinbam[3]

Abstract

A fully digital phase locked loop used as phase tracking circuit in GPS receiver is designed and simulated using VHDL. The PLL has no off chip components and it is made from standard cell libraries. The design is, therefore portable between technologies as an IP block. The work mainly aims at area and power efficient design of ADPLL such that they can be used in GPS for mobile systems. In addition, the next version of this all-digital PLL is described. A new time-to-digital converter with higher resolution is designed for the improved PLL. An improved digitally controlled oscillator with low power consumption is also suggested.

Keywords: *All digital phase locked loop (ADPLL), Global Positioning System (GPS) receiver, Phase frequency detector (PFD), Digitally Controlled Oscillator (DCO), Time to digital converter.*

1. Introduction

Global positioning system is a satellite-based navigation system consisting of 24 orbiting satellites that are orbiting in space eleven thousand miles from Earth. Each satellite transmits a message containing three pieces of information, the satellite number, its position in space and the time at which the message was sent [1]. The GPS receiver reads the message and saves the information. Fig 1 shows the block structure of GPS receiver. The receiver itself consists of two functional blocks, the front-end and the code/carrier tracking loops. The front-end performs down-conversion of the received signal from L1-band to an Intermediate frequency. The samples are digitized with a three-level discriminator. The digitized samples are tracked by the tracking loop.

The tracking block is used to find the phase transition of the navigation data. To track a GPS signal two tracking loops are necessary. One loop is used to track the carrier frequency and is referred to as the Carrier loop. The other is used

[1] Lecturer, Department of Electronics Engineering, MIT Campus, Anna University, Chennai-44, srimoorthi@annauniv.edu
[2] ME Student, Department of Electronics Engineering, MIT Campus, Anna University, Chennai-44, kspavithra@gmail.com
[3] Prof & Head, Department of Media Sciences, CEG, Anna University, Chennai-25

DESIGN AND OPTIMIZATION OF ON CHIP SPIRAL INDUCTOR FOR SILICON BASED RF IC's

Genemala Haobijam[1], Roy Paily[2]

Abstract

This paper presents an efficient method to determine the optimum layout parameters of a spiral inductor of any inductance value that results the highest quality factor possible in a given technology. The figure of merit (FOM) of any inductance (L) is given by its quality factor (Q), self resonance frequency (f_{res}) and optimum frequency (f_{max}). The FOM has numerous tradeoffs with the layout parameters such as number of turns (N), spiral track width (W), track spacing (S), outer diameter (D_{out}), inner diameter (D_{in}) and the technological parameters such as substrate resistivity, insulator thickness, conductor thickness and resistance. The proposed method solves the design complexity by deciding these performance controlling parameters based on a lumped physical model. The main prospect of the algorithm is to ease the design and optimization of a number of inductors of different L values that meets the same area limits. The algorithm fulfills this by determining the range of inductance that can be realized within an area bound by varying N and W and thus the layout parameters bounds to realize any desired value of inductance is easily obtained and within these bounds the algorithm finds the optimum layout parameters that gives the highest Q.

Index terms: Spiral inductor, Q factor optimization.

1. Introduction

On chip spiral inductors are extensively used in monolithic radiofrequency integrated circuits (RFIC's) such as voltage controlled oscillators (VCO's), low noise amplifiers (LNA's) and passive element filters. The performance of these RF cells is also governed by the quality of the passives in addition to the active devices. Of the RF passive components, spiral inductor is the most crucial passive component [1]. On chip spiral inductors are characterized by (i) quality factor Q, (ii) optimum frequency f_{max} at which Q reaches its maximum value Q_{max}, and (iii) resonance frequency f_{res} at which the inductor behaves like a parallel RC circuit in resonance and is far from behaving as an inductor [2]. These characteristics of the spiral inductor is determined by its geometrical or layout parameters such as number of turns (N), spiral track width (W), track spacing (S), outer diameter (D_{out}), inner diameter (D_{in}) and the technological parameters such as substrate resistivity, insulator thickness, conductor thickness and resistance. The layout parameters are shown in Fig.1. The performance of

The authors are with the Department of Electronics and Communication Engineering, Indian Institute of Technology Guwahati, Assam-781039, India.
email : [1]genemala@iitg.ernet.in, [2]roypaily@iitg.ernet.in

A NOVEL UNIFIED FRAMEWORK FOR FUNCTIONAL VERIFICATION OF PROCESSORS USING CONSTRAINT SOLVERS

Debi Prasad[1], Archana Rai[1], Karthik Venkatraman[1], Senthil Kumar[1], V Kamakoti[1], Kailasnath S Maneperambil[2] and Vivekananda M Vedula[2]

Abstract

With the advent of modern performance-driven processors, the concept of functional verification has transcended from a mere verification of the Instruction Set Architecture (ISA) towards verification of micro-architectural features, whose complex functionality accounts for the performance of the processor under test. In other words, functional verification does not stop with testing whether a set of assembly programs execute correctly, but proceeds to verify, for example, the effectiveness of a cache-replacement policy. This implies a need to generate directed tests that create specific micro-architectural events. An issue that would be of great interest to the processor verification community in the coming years would not only be to generate tests that verifies micro-architectural features of individual modules, like Cache, TLB etc, but also that would verify the complex interaction among them. In this paper, we present a novel unified framework for the functional test generation for processors. The framework can be used to generate directed test for functional verification of processors, at different levels, namely, the Instruction Set Architecture to Micro-architecture, and also combinations of them. A Constraint Solver based approach is employed in the framework. The effectiveness of the framework is demonstrated by developing the same using the ILOG Constraint Solver and plugging-in Cache and TLB models into it.

1. INTRODUCTION

Functional Verification is widely recognized as the bottleneck of the hardware design cycle. With the ever-growing demand for greater performance and faster time to market, coupled with the exponential growth in hardware size, verification has become increasingly difficult. The recent emergence of hardware verification languages and comprehensive environments designed to automate the functional verification process has significant effects on the simulation-based methodology for verification. Engineers typically use these environments to verify ASICs, SoCs, and unit-level components in a processor. Using such environments to verify large processors like x86, PowerPC etc. still requires significant manual effort.[1]

[1] Reconfigurable and Intelligent Systems Engineering Group, Dept. of Computer Science & Engg, IIT Madras, Chennai [2] Validation and Test Solutions, Intel Corporation, Austin

STUDY AND CHARECTERIZATION OF GaAs AND InP DEVICE FOR NANOAPPLICATIONS.

E.N.Ganesh[1], P.K.Singh[2], Lal Kishore[3]

Abstract:

Compound semiconductors are well known for its high speed due to its higher mobility. Indium Phosphide and Gallium Arsenide are the compound semiconductor material considered in this paper for its study and characterization. Indium Phosphide MIS devices can be fabricated and its characteristics are studied. Here Indium Phosphide MIS capacitor is used as test vehicle for fabrication of other MIS devices. We noted down its breakdown voltage and leakage current. MIS devices can be used for fabricating Bio-electrodes in Medical applications. Then we have simulated GaAs Field Effect transistor devices as switches or Inverters. The devices made up of GaAs can be used as Logical elements in Machine controlled systems. We considered two examples of Machine Controlled system and can be modeled as Logical elements. GaAs NOT, NAND, NOR Circuits are drawn and simulated and its characteristics are noted down. We conclude that Compound semiconductor devices have higher response time and less power compared to silicon.

KEY WORDS – GalliumPhosphide,Indium Phosphide,Metal Insulator semiconductors,Compoundsemiconductors.

1. INTRODUCTION

Gallium Arsenide and Indium phosphide are compound semiconductor material for its high speed and high-density integrated circuits. GaAs and InP are direct band gap material. Therefore it can be used for fabricating high-speed Electronic devices. The wider energy gap of GaAs (1.43 eV) and InP (1.34 eV) makes it attractive for operation at higher temperatures. GaAs and InP has high electron mobility (4500 cm^2 / V.sec)[2] and high velocity overshoot effects than Silicon. This paper discusses about devices made of InP and GaAs.

1.1 INDIUM PHOSPHIDE

Metal insulator Semiconductor capacitor made of Indium phosphide is fabricated and its characteristics are studied. Detail fabrication steps are listed and the MIS structure is tested for its I-V and C-V characteristics. From the characteristics Breakdown voltage, Leakage current, Interface state density at the surface can be found. Metal Insulator semiconductor devices are used to fabricate Bio-electrodes for Nano - Medical Applications. We fabricated capacitor type device and studied its characteristics. The study gives ideas about other MIS device fabrication.

enganesh50@rediffmail.com

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A NOVEL CMOS COMPATIBLE THREE TERMINAL 3D TUNABLE MICRO INDUCTOR

V. Siva Rama Krishna[1], K[1].Jayant and Navakanta Bhat
National MEMS Design Centere
Electrical and Communication Engineering
Indian Institute of Science
Bangalore -560012

Abstract

This paper presents a novel design of a CMOS compatible tunable three dimensional inductor. The inductor makes use of series connected cantilevers switches to complete one loop of a solenoid. Tunability is achieved by varying the number of turns of the inductor by adding more cantilever based switches in series. The inductors were fabricated using Poly MUMPs [1] process and natural frequency measurements were done using a Laser vibrometer to test the functionality of the device.

1. Introduction:

The world of RF communications demands a high quality inductor. It would be an added advantage if tunability is also there along with high Q. Tunable inductors provides wide range oscillation of VCO and wide impedance matching and so on. On-chip planar inductors have low quality factor due to losses caused by skin effect, proximity effect and substrate currents. Removing the substrate under the coil removes the eddy current loss but the skin effect loss is not taken care of [2].Out of plane inductors with the coil axis parallel to the surface offers the solution to both the problems[3]. Fig.1 shows the magnetic flux and the current density in conventional inductors and the out of plane inductors. The bulk of the magnetic flux runs above the substrate reducing the eddy current. Skin and proximity effect pushes the current to the outer surfaces rather than the edges. Increasing the width of the coils will reduce the resistance thereby the losses. This paper proposes a 3D inductor which can be used in two ways. The first way is to use it as a tunable inductor. The tunability is achieved by the use of cantilever beams. Although variable inductors based on cantilever DC switches have been done [4], the structure proposed is made of cantilever lever

[1] Contact : V.Siva Rama Krishna, Ph.D student, Dept. of E.C.E, I.I.Sc.
e-mail: svanjari@ece.iisc.ernet.in

DESIGN AND POWER-PERFORMANCE OPTIMIZATION OF A LOW LEAKAGE SERIAL CAM

N. N. Mojumder, A. Dandapat, D. Mukhopadhyay[1]

Abstract

The Content Addressable Memory (CAM) is a class of memory that allows access by data instead of by physical address. On a read access to a CAM, embedded into a processor cache, each word is compared in a broadcast mode, to see if it matches the requested data; thus requiring only one access. Due to their parallel pattern matching property, CAMs are gaining increasing importance over Random Access Memory (RAM) in recent years, though design complexity and power consumption continue to remain the major drawbacks.

The challenge in the design of a CAM cell is to reduce leakage power in its compare circuitry without sacrificing the speed. This paper describes a novel high-performance low power design of Serial CAM block using Dual-Threshold CMOS (DTCMOS) technique, Transmission Gates (TG), Transistor Stacks and an efficient Match Adaptive Architecture. In this design, for high speed and low power operation, we have used four separate, though not independent techniques. Replacing pass transistors by TG, including transistor stacks in the compare circuitry and assigning appropriate threshold voltages with dual threshold technique have been found to reduce the Power Delay Product (PDP) of the basic serial CAM cell by as much as up to 30%. Switching to a unique Match Adaptive Architecture further improves this Power-Performance of the CAM block significantly as compared to the conventional configuration.

Index *– Stack Transistor, Dual Threshold CMOS, TG, PDP, Match Adaptive Architecture*

1. Introduction

The 10-transistor (10-Tx) Serial CAM configuration shown in Fig.1 is the basic building block in cache memory organization [1]. Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all kinds of search applications. Unlike a RAM, which has simple storage cells, each individual memory bit in a CAM must have its own comparison circuit to detect a match between the stored bit and the input bit.

[1] Dept. of Electronics and Telecommunication Engineering, Jadavpur University, India

GAS SENSOR INTERFACE ASIC ON 0.7µm CMOS TECHNOLOGY

Shobi Bagga [a] Navakanta Bhat [b] S.Mohan [a]

ABSTRACT

A high accuracy wide dynamic range front end for gas sensor is presented. We have designed the sensor readout circuit working on the principle of the resistance to period conversion and demonstrate an excellent linearity (<0.1%) over third order of change in sensor resistance. For improving the sensitivity of the sensor we have also designed the on/off based temperature control circuit, which drives the off chip power transistor to control the temperature of sensing element.

Keywords: *Gas sensor, temperature control circuit, linearity, power transistor*

I. Introduction

CMOS based gas sensor are becoming attractive for variety of applications [1].We are developing LPG gas sensor based on tin oxide based semiconductor .This sensor is based on the principle that its resistance decreases in the presence of reducing gases such as LPG. However this sensor becomes active only at high temperature such as 300^0 C .The value of the sensor resistance (Rsens.) is given by the following equation

$$Rsens = Rbi + \Delta Rbi + \Delta Rgas$$

where Rbi is the baseline resistance which mainly depends on the fabrication technique, ΔRbi is the deviation from the baseline due to technological and aging spread & temperature and the resistance variation ΔRgas, which depends on gas concentration, negative for most gas types. Its value can be as large as a couple of decades from the actual baseline. Depending on sensor type, technology spread and sensor age, the baseline can vary from a very low value, i.e. KΩ range to MΩ range .The large dynamic range of change in Rsens requires appropriate circuit technique. For instance logarithmic approach can be used but it introduces some nonlinearity, which reduces the precision of resistance reading [1].

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a Department of Instrumentation, Indian Institute of Science,Bangalore-12
b Department of ECE, Indian Institute of Science,Bangalore-12
Email: sbagga@isu.iisc.ernet.in

GENERAL PURPOSE CAPACITIVE SENSING CIRCUIT USING CORRELATED DOUBLE SAMPLING

Sandeep K, Chaitanya K and Navakanta Bhat

Abstract

This paper introduces a differential capacitive sensing using correlated double sampling technique and a novel on chip offset reduction circuit using capacitance array. This capacitance array can also be used to overcome any capacitance mismatch in the bridge sensing circuit. The minimum resolution obtained using this sensing circuit is 1ppm (Part Per Million) of the base capacitor. The minimum differential capacitance change which can be obtained using the capacitance array is 0.5fF and ranges up to 2pF. The circuit is implemented using 0.7µ AMIS technology and has been submitted for fabrication.

Keywords: Capacitive sensing, Capacitor Array, Correlated double Sampling.

1. Introduction

Capacitance Transducers serve as an interface in various MEMS-CMOS sensors such as accelerometer, gyroscope, and pressure sensors. These transducers generally result in differential capacitance change as a function of displacement of the sense element. Because the differential capacitance variations ΔC is very small, normally in the range of few attoFarad to hundreds of femtoFarad, the effect of parasitics, 1/f noise, and dc offset of the amplifier has to be reduced. Correlated double sampling can remove 1/f noise and amplifier offset, charge injection and kT/C noise due to switching operations [2] [3].

The paper is organized as follows. In Section 2, we discuss the system level block diagram of the CDS capacitive sensing circuit. Section 3 & 4 deals with circuit level design and implementation of the CDS sensing circuit and capacitor array. Section 5 provides the simulation results and also on-chip testability plans. Finally we summarize the results obtained in Section 6.

Microelectronics Lab , Indian Institute of Science , Bangalore - 12

Critical Path modeling for Dynamic Voltage Scaling (DVS) in Low Power Applications

Bishnu Prasad Das[1], Bharadwaj Amrutur[2], H.S. Jamadagni[1]

ABSTRACT

Dynamic Voltage Scaling requires a model of the critical path to allow the proper setting of the supply voltage to meet a target frequency. In this paper, we propose a new technique to model the supply and delay relationship of a critical path which is based on Gaussian Radial Basis Functions (RBF) neural network. This modeling technique is able to successfully capture the process and temperature variability even at the granularity of individual transistors. The accuracies are comparable to SPICE, but with much less computational requirements. As a demonstration, we model a ring oscillator using the RBF network, and solve the problem of finding the optimum voltage for a target frequency across parameter variations.

1. INTRODUCTION

Dynamic voltage scaling has recently gained widespread use as a low power technique for digital designs, wherein the supply voltage for the circuit block is dynamically adjusted to be the minimum possible value such that the performance target is still achieved, while minimizing power dissipation [Nielsen (1994), Wei (1996), Gutnik (1997)]. The basic philosophy here is to leverage extra performance margin and use it to get back some power savings. One of the key problems in this approach is to determine the minimum supply voltage such that the circuit block meets the target delay constraint under all process and environment conditions. This problem is exacerbated in deep submicron technologies as the inter-die and intra-die variations have increased with process scaling [Borkar (2003), Bowman (1999)]. There are two basic approaches to solve this problem. In one, a model of the critical path of the circuit block is constructed and used in a feedback loop with the power supply controller [Nielsen (1994), Wei (1996), Gutnik (1997)]. The delay of this model path is continuously measured to adjust the power supply controller to output the desired voltage. A critical assumption in this approach, which is also its most serious limitation, is that the model path tracks the critical path delay of the circuit block. But a well designed circuit block might have many critical paths. Besides in a large chip with temperature gradients, different paths might become critical at different voltage values and this might also vary from chip to

[1] Center for Electronics Design and Technology, Indian Institute of Science, Bangalore 12, India {bpdas , hsjam}@cedt.iisc.ernet.in
[2] Electrical Communication Engineering Department, Indian Institute of Science, Bangalore 12, India amrutur@ece.iisc.ernet.in

DESIGN AND STUDY OF AN ELECTROSTATIC TORSION MICRO ACTUATOR FOR BEAM STEERING IN HORIZONTAL PLANE

D. Vijaya Bhargava and Roy P. Paily[1]

We have proposed an Electrostatic Torsion Micro actuator for beam steering in the horizontal plane. The design and simulation of the proposed micro actuator structure is carried out in INTELLISUITE software for MEMS. To facilitate beam steering in the horizontal plane, a novel fabrication methodology within the constraints of planar process steps is developed. We have employed a simplified model for calculating the pull-in voltage and pull-in angle of an electrostatic torsion micro actuator. Pull-in analysis of the optimized structure is carried out and pull-in voltage of about 40V and pull-in angle of about 3.14º are obtained.

Key Words— *Electrostatic, torsion, actuator, micro fabrication, pull-in voltage, beam steering.*

I. Introduction

In the MEMS (Micro Electro Mechanical Systems) technology, the powerful principles of Electronics and Mechanics are combined together, to realize miniaturized products for sensing and communication. The micromachined electrostatic micromirrors have been demonstrated in barcode reader, confocal optical microscope, scanner, laser printer etc [1] where beam steering is necessary. In optical storage also, beam steering mechanism is essential for read/write operations of the CD or hard disk. This eliminates the need for the conventional methods like rotating the disk. Beam steering is also significant in laser communication, for example in providing a wireless optical communication link between two aerial vehicles. The forces required for the mechanical movement of the mirror can be obtained using electrostatic, magneto static, piezoelectric or thermal designs. Electrostatic actuation is the most

[1] Department of Electronics and Communication Engineering,
Indian Institute of Technology Guwahati, Guwahati-781039, India.
email: roypaily@iitg.ernet.in

FAULT TOLERANT FPGA USING REDUNDANT COLUMNS

Neeraj Goel and Kolin Paul[1]

Abstract

Fault tolerance techniques are important to increase the yield of the VLSI chips in advanced fabrication technologies. In regular structure like FPGA, redundancy is commonly used for fault tolerance. Most of the techniques found so far in literature talks about software based change in configuration data. Here in this work we present a solution in which configuration bit stream of FPGA is changed by a hardware controller that is present on the FPGA chip itself. The technique uses redundant columns for replacing faulty cells. Two variation of the technique is presented and thereafter a qualitative analysis of the tradeoffs is done.

1 Introduction

As the technology is shrinking, the defects in VLSI chips are increasing thus decreasing the yield. Aim of this work is to increase the yield by designing fault tolerant FPGA. FPGAs have a uniform fabric, consist of programmable logic units (which are referred by cells in this paper) and programmable interconnects. Placement and routing tools map any circuit (net-list) to the fabric optimally. Because all cells are identical in nature, if one cell is found defective then other cells can be used in place of it. This approach is generally called redundancy based approach and is the base of this work. Redundancy based approaches, for fault tolerance, are quite old techniques in FPGA and memories as discussed in Hatori et al(1993) and Stapper (1980). The difference between memory and FPGA architecture is routing complexity. FPGA have a complex routing structures where interconnects are generated by time consuming place and route process. For any spare row changing routing is the prime concern.

Spare column based technique has been proposed by Huang et al (2001). In the technique spare column is used by place and route tool given the fault locations. In this work fine grain detail about the new routing after the column shifting was not given. In another work by Yu and Lemieur (2005), fault tolerant interconnect structure was built. In their work switch box interconnect was modeled and faults in interconnects were corrected by spare routing channels which were not used by place and route tool. Rahul Jain et al (2006) take defect map as input to place and route tool. Tool does the placement in such that defective cells are not used. In another approach by Doumar et al (1999) EDA tool will take a generic defect map (which may be different then real defect map of the chip) and generate place and route according to that defect map.

We are proposing a technique in which hardware controller on FPGA will take defect map and configuration file as input. We are using spare columns

[1] Contact: neeraj,kolin@cse.iitd.ernet.in, Dept of Comp Sci, IIT Delhi

FPGA Implementation of a new hardware architecture for Smoothing Two Dimensional Images Corrupted by Noise

N.Venkateswaran[1] and Y.V Ramana Rao[2]

Abstract

This paper presents new hardware architecture for smoothing an image corrupted by noise. An efficient hardware implementation of a mean filter is also presented. It is a very common operation in image smoothening where each pixel is replaced by an average of few nearby pixels. The design is carried out for a specific of window size of 3X3. The sum total of all input pixels within the window is divided by nine. The computation of the average is carried out by our simple and fast architecture based on polynomial division. The architecture can be further pipelined to optimize for speed. The performance of the proposed approximation is analyzed by using it in the spatial average filtering of an image corrupted by Gaussian noise and comparing the filtered image with that in which accurate division by nine is used. The design is synthesized for a Xilinx Virtex II FPGA and the performance results are given.

Keywords:
Division operation, spatial averaging, image processing

I. Introduction

The spatial averaging filter is a non-linear filter that has been used successfully in a variety of smoothing transformations. Its strength lies in its ability to filter out noise caused by transmission lines or quantum noise associated with image acquisition, without destroying the properties of the underlying signal. It spatial averaging filter is computationally simple and easy to implement in hardware. An alternative to this filter is a weighted moving average filter and the median filter, which are more complex. All these filters perform relatively similar in performance for detail preservation, edge preservation and overall visual quality.

Spatial averaging filters are used in the suppression of gaussian/uniform noise in images [1]. In general, given an input sequence x1, x2, x3, · · ·, of pixel values, with a window of size 2N + 1 centered on the i^{th} value as Wi ={xi-N, xi-N+1, · · · , xi, · · · , xi+N-1, xi+N}. The output of the smoothing filter, yi, is thus the average of Wi;

Contact Information:[1]*Department Of Electronics and Communication Engineering.* Sri Venkateswara College Of Engineering., Sriperumbudur, India. 602105.
[2]*Department Of Electronics and Communication Engineering. College of Engineering, Anna University,Chennai-25, India*
nvenkat@svce.ac.in, yvramana_rao@hotmail.com

A Novel Low Power Bus Encoding Technique for Minimizing RGB Transitions for LCD Display of Digital Camera

J.V.R. Ravindra*, K.S. Sainarayanan*, M.B. Srinivas*

Abstract

This paper presents an efficient low-power bus encoding technique which is suitable for minimizing the RGB transitions for Liquid Crystal Display (LCD). In particular, this paper focuses on interfaces that are compliant to the CMOS sensor and LCD, in which the three color channels (R, G and B) are parallely, transmitted to achieve high bandwidth. Since significant amount of power is dissipated in LCD interface, the proposed encoding technique aims at minimizing adjacent transitions of the data. It has been found that by applying the proposed coding scheme, the energy saving of around 32% is achieved, with respect to a plain transmission for 24, 48 bit pixel data. The algorithm has been applied to USID image benchmarks and achieved a 32% power savings.

Keywords

Liquid Crystal Display (LCD), Thin Film Transistor (TFT), Low Power, Bus Coding, Self and Coupling Transitions, VLSI.

1. Introduction

Due to the high computational power of the processor cores and the huge amount of SRAM memory [1], the Liquid Crystal Display (LCD) system is still one among the most technically demanding component, among the modern multimedia devices. Besides the high amount of power consumed by the LCD panels, a significant fraction of the entire LCD system's power budget is taken by the LCD bus [1, 2]. Liquid Crystal Display is intrinsically a non-power-manageable resource. It must be continuously refreshed, and shutting it down cannot be done without significant penalty in performance, especially in image quality. In this scenario, design techniques that facilitate the reduction of the switching activity of digital LCD buses become more promising than those for parallel on/off-chip memory/processor buses, which have been studied in [2]. Moreover, LCD bus capacitances are in fact much larger than that of typical on-chip buses. All standard digital LCD interfaces use a parallel connection to communicate with the panel, mostly to minimize electrical effects occurring during the transmission of data on a flat cable at frequencies in the range required by typical LCD displays. A suitable encoding solution for LCD buses must thus be focused around parallel communication channels. This constraint rules out most of the existing techniques for energy-efficient bus encoding, which are focused on parallel buses.

The video information for images that are to be displayed on the LCD is stored in the frame buffer in a bitmapped manner. The video controller reads the information from the frame buffer and drives the LCD to display the corresponding image. When the color indices from the pixel buffer are sent to

*Center for VLSI and Embedded System Technologies,
International Institute of Information Technology,
Gachibowli, Hyderabad 500 019, India.
Email {ravindra, kssai @research.iiit.net}, srinivas@iiit.net

AN EFFICIENT FPGA IMPLEMENTATION OF A CRYPTOGRAPHIC HASH ALGORITHM BASED ON CELLULAR AUTOMATA

Roshni Chatterjee[1] and Dipanwita RoyChowdhury[2]

Abstract

With collisions being announced for the most widely used hash algorithm SHA and the widespread use of security algorithms in hardware devices like PDAs, there has been an increasing demand for a secure cryptographic hash algorithm that has an easy and efficient VLSI implementation. This has inspired researchers to propose hash algorithms oriented towards easy hardware implementation, one of which is CAHASH, a hash algorithm based on Cellular Automata. The key contributions of this paper are as follows: (a) Identification of a weakness in CAHASH (b) A proposed modification in CAHASH to remove this weakness, and (c) An efficient FPGA-based implementation of the modified algorithm. Due to the use of pipeline and efficient Galois field multiplier blocks, our implementation outperforms some of the best hardware implementations of standard hash algorithms, like SHA. In addition, due to the regular structure of Cellular Automata, the area overhead for our implementation is less.

Keywords: Hash Algorithms, Cellular Automata, Galois Field Multiplication, FPGA, pipeline.

1. Introduction:

Over the years, numerous cryptographic hash algorithms [5,9,11] have been designed. However, recently there has been a demand for an efficient VLSI implementation of a new, secure hash algorithm. The reasons are: (a) The most widely used hash algorithm SHA[9] has been attacked in 2004 and 2005 [3,12,13,14] , thereby evoking the need to propose a new secure hash algorithm. (b) Due to the increased use of cryptographic hash algorithms in devices like PDAs, simple, efficient and easily implementable hash algorithms are being looked for.

The design of popular hash algorithms like MD5 and SHA do not target an efficient VLSI implementation. Therefore, designers have proposed hash

[1] MS Student, Department of Comp. Sc & Engg, IIT Kharagpur, India, roshni@cse.iitkgp.ernet.in
[2]Associate Professor, Department of Comp. Sc & Engg, IIT Kharagpur , India, drc@cse.iitkgp.ernet.in

A POWER EFFICIENT ARCHITECTURE FOR 2-D DISCRETE WAVELET TRANSFORM

Rahul Jain[1], Preeti Ranjan Panda[2]

Abstract

The Discrete Wavelet Transform (DWT) forms the core of the JPEG2000 image compression algorithm. Since the JPEG2000 compression application is heavily data-intensive, the overall power dissipation is dominated by read and write operations in the memory subsystem. In our proposed architecture, low power has mainly been achieved by optimizing the memory architecture and the data access pattern. The proposed architecture is a Low-Power Z-Scan method. Different memory subsystem optimization techniques such as data access and computation restructuring, memory bank partitioning, and custom memory architectures are explored to arrive at a power-efficient DWT architecture.

1. Introduction

JPEG is the first international image compression standard for continuous-tone still images. JPEG2000 is the newest standard from JPEG committee. Discrete Wavelet Transform (DWT) is at the core of the JPEG2000 structure [1]. The cost of 2D-DWT is dominated by memory size and memory bandwidth. DWT is performed on a much bigger image tile as compared to 8x8 image block in DCT. DCT requires 64 bytes of on-chip storage to store the 8x8 block. On the other hand, direct 2-D DWT architecture computes the row-wise 1-D DWT and stores it in a buffer and then computes the 1-D DWT column-wise. If the intermediate values are 16 bit, than for a 512x512 image tile, the on-chip memory requirement is 512KB. Because of this huge on-chip memory requirement, the intermediate result is stored off-chip and read back again. This increases the power as well as the delay. Memory access is responsible for a major fraction of the power consumption. Hence optimizing the memory access and architecture is very important in case of DWT architecture.

1.1 Memory Architecture Optimization

In current system-on-chip (SoCs), embedded memories occupy almost 70% of the chip as predicted by Semiconductor Industry Association (SIA), ITRS 2000. In the hardware implementation of data-intensive algorithms like 2D-DWT, the energy dissipation due to data storage and transfers accounts for almost 80% of the total power budget [2]. This has moved the focus to memory performance and power. Since embedded memories greatly reduce the energy and delay [3],

[1] CoWare India Pvt Ltd, Noida : rahul.jain@CoWare.com
[2] Indian Institute of Technology, Delhi : panda@cse.iitd.ernet.in

DESIGN AND IMPLEMENTATION OF MORPHOLOGICAL OPERATIONS AND MEDIAN FILTER FOR IMAGE PROCESSING APPLICATIONS

Kapadia Payal Rohit[1], Raj Singh[2], Ravi Saini [3]

Abstract

The objective of this work is to design median filtering and morphological operations (dilation and erosion) for image processing applications using rank-order filter and implementing the same on FPGA. From these basic morphological operations, other operations such as opening, closing and edge-detection are implemented. All these functions are implemented using 3x3 and 5x5 structuring element. Data size can be either 8-bit or 16-bit. Simulation and synthesis for image sizes up to 2048x2048 have been successfully done and frame-rate required for digital video image processing is achieved. For the implementation of rank-order filter, merge-sort sorting architecture and moving-window architecture is designed for both 3x3 and 5x5 structuring element. In this architecture, a 256x16-bit and 256x8-bit synchronous FIFO is designed so as to reduce the amount of logic blocks utilization by using available BlockRAMs on target FPGA.. Image-to-file and file-to-image conversion routines were written in software for processing the image in VHDL code and for viewing the processed image.

Keywords: *Morphology, Image Processing, VLSI Design*

1. Introduction

Digital image processing is mainly used to improve the visual appearance of an image to a human viewer, to know about image features and structure that is either edges or internal structure. Morphology is mainly used for segmentation, representation and description e.g. Gonzalez and Woods (2001). In this paper, we have implemented dilation, erosion, and edge-detection using results of dilation; edge-detection using result of erosion; median filtering; image opening and image closing operations on a FPGA.

2. Morphology and its Operators

The term, morphological image processing, refers to a class of algorithms that is interested in the geometric structure of an image. Morphology can be used on binary and grayscale images. It is useful in many areas of image processing, such as skeletonization, edge detection, restoration, and texture analysis e.g.

[1] M.Tech Student of Nirma University, Ahmedabad worked on during stay at CEERI
[2] IC Design Group CEERI , Pilani
[3] IC Design Group CEERI, Pilani

A NOVEL LO CIRCUIT FOR SUB-HARMONIC MIXER

R.N.Biswas, C.Parikh, G.P.Krishna Kishore [1]

Abstract

Sub-harmonic up and down conversion mixers have been simulated with sinusoidal, triangular and trapezoidal LO waveforms on 0.18µ CMOS technology. All the LO waveforms showed a 40 dB carrier suppression and a 60 dB side band suppression with respect to desired band at the output of the mixer. The contributions of this paper are derivation of a theoretical model for sub-harmonic mixer which proves that any periodic odd symmetry waveforms can be used as LO to Sub-harmonic mixer as against the sinusoidal LO in the previously published papers and a novel octet-phase LO generating circuit has been designed with CMOS inverters. The proposed circuit generates symmetrical trapezoidal LO waveform with lower power consumption and less transistor sizes. Performance of sub-harmonic mixers using trapezoidal octet-phase LO waveforms has been shown to be quite comparable with sub-harmonic mixers using sinusoidal LO waveforms.

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1. Introduction

Direct Conversion (DC) RF transceiver is the enabling technique for the next generation cellular and personal communication devices striving for miniaturisation, long life of battery and cost effectiveness. It was argued that [1] DC architectures are suitable for wideband signals, which contain less information at low frequencies to over come flicker noise problems. DC architectures are also less susceptible to quadrature LO errors if spread spectrum techniques like WCDMA are used. Existing techniques of DC suffer from undesired LO radiation from the receiver, which falls in the same receive band of the cellular system. This leads to distortion in the signal received by the mobile users in the close proximity [2], [3]. Various techniques are proposed to avoid the strong LO (carrier) signal in the mobile systems [4]. One such technique is the Sub-Harmonic (SH) mixer which uses an LO operating at half of the required carrier frequency, and generates the required carrier frequency by systematic switching of the transistors by four balanced quadrature phases of the LO signal [5]. Various methods are proposed [4] to generate the quadrature phases of the LO like poly-phase filters [6], [7] and ring oscillators [4]. It was

[1] Contact Information:
Prof. R.N.Biswas, DA-IICT, Gandhinagar rn_biswas@da-iict.org
Prof. C.Parikh, DA-IICT, Gandhinagar chetan_parikh@da-iict.org
G.P. Krishna Kishore, ATLAB Inc., Republic of Korea gunturikishore@gmail.com

Exact Method for Estimating Expected Settling Power in Sequential Circuits

Diganchal Chakraborty[*], Partha P. Chakrabarti[*], Pallab Dasgupta[*]

Abstract

A huge amount of power is dissipated in a sequential circuit during when various flip flop outputs change their values and several other internal nodes settle at specific values following the arrival of a clock pulse. This paper presents an exact method of estimating the expected amount of this power using symbolic simulation. State transition probabilities, which are required by this method, are computed by implicitly solving the system of Chapman-Kolmogorov equations obtained from modeling the state transition system of the circuit as a discrete time Marcov chain. The conducted Monte-Carlo simulations on the ISCAS'89 benchmark circuits show that the proposed method is accurate up to 2-3% and considerably faster.

Keywords: Symbolic simulation, event, Markov chain, Stationary state probability.

1. Introduction

Design for low power has become an important area of research in today's electronics industry. The continuous growth in chip density, increasing complexity of designs and the advent of portable devices has created a demand for new and faster tools for low power synthesis. Besides efforts in low power synthesis, a lot of effort has been directed towards inventing tools for fast and accurate estimates of power for various circuit implementations.

Usually, in case of sequential circuits, the normal mode of operation is to fix the values at the primary inputs long before the clock pulse comes, so as the circuit gets stabilized before the arrival of clock pulse. With the arrival of clock pulse some of the flip flops may change their values and these values may get propagated to several other internal nodes in the circuit very fast which may cause considerable energy dissipation within a very short period of time. We term this energy per clock period as the settling power of the circuit. Expected settling power (ESP) is the expected value of settling power over all possible inputs and all possible transitions at the flip flop outputs in the circuit.

[*] Department of Computer Sc. & Engg, IIT Kharagpur - 721302
{diganchal,ppchak,pallab}@cse.iitkgp.ernet.in

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A FULLY ON-CHIP AGC FOR RF-TRANSCEIVERS COMPLYING LR-WPAN

Harsh T[1], Abhay N.A[2], Tawade R[3]
[1]Lecturer, SIT Lonavala. [2]Asst Prof BVP Pune. [3]Senior Lecturer, SCOE Pune

Abstract

This paper presents a low-voltage, low-power design for the automatic gain control of RF Transceivers. Our design is more suitable for RF applications for low data rate such as home automation, interactive devices, industrial monitor and control. Mobile radio handsets an on-chip circuit and sensor applications require measuring the received signal-strength and this received signal is used as the control voltage for varying the gain of VGA, to regulate the transmitted power level, and to determine cell-handoff. There by, controlling the gain of transceiver.
The architecture of VGA employed is determined by the optimal power consumption for a specified speed, overall gain, and accuracy. Each VGA cell comprises a differential pair with a common-mode feedback and four cross-coupled control transistors for low voltage operation. VGA working at an IF frequency of 2 MHz is chosen for our application. Full-wave current rectification and summation are employed in the RSSI circuit to achieve high precision. Using a single 1.8-V supply voltage, measured results for RSSI demonstrate the input dynamic range is larger than 80 dB. The noise Figure at a maximum gain of 60dB is 6dB.The prototype is implemented using a 0.18u CMOS technology and occupies an active area of 0.8 Sq mm. The power dissipation is 6mW.This on chip architecture is designed and implemented for RF Transceivers complying LR-WPAN.

Keywords
Variable gain amplifier (VGA), AGC, RSSI, CMOS, Wireless Communication,, Field Effect Transistor (FET), Full Wave Rectifier (FWR), System-On-Chip (SOC)

1. Introduction

VGA circuits are employed in many applications in order to maximize the dynamic range of the overall system [1]. These are often employed in imaging circuits, hearing aids, disk drives, and in virtually all-wireless communication systems [2]. The automatic gain control (AGC) loop is needed in wireless systems since the received signal power of all communication systems has a wide dynamic range [3]. In order to keep the communication systems working under these conditions, a VGA is typically employed in a feedback loop to realize the AGC circuit [4], whose output signal has a fixed magnitude for different input signal strengths [5].
LR-WPAN is a new wireless networking standard, which will enable a whole new set of radio products for low cost and low power [1]. This standard is

WAVEFORM ANALYSIS AND DELAY PREDICTION FOR CMOS DRIVEN *RLC*-MODELED VLSI INTERCONNECT

B.K.Kaushik, S.Sarkar* and R.P.Agarwal**

Abstract
This paper deals with the problem of estimating the performance of a CMOS gate driving *RLC* interconnect load. The widely accepted model for CMOS gate and interconnect line is used for the representation. The CMOS gate is modeled by an Alpha Power law model, whereas the distributed *RLC* interconnect is represented by an equivalent π-model. The output waveform and the propagation delay of the inverter are analytically calculated and compared with SPICE simulations. The analytical driver-interconnect load model gives sufficiently close results to SPICE simulations for two different cases of slow and fast input ramps. For each case of stimulations the model gives an insight to four regions of operation of the CMOS gate. The voltage waveform at the end of an interconnect line is obtained for each region of operation. The SPICE and analytical results for the output voltage waveform and propagation delay matches very closely.
Keywords—Interconnect Modeling; Distributed RLC Interconnect; Propagation delay.

1. Introduction

Predicting accurately the waveform shape and propagation delay in a driver-interconnect load model has been an important design perspective since long time. Previously, Chatzigeorgiou *et al.* [1], analyzed distributed *RC* interconnect load represented as *CRC* π-model driven by CMOS gate, but inaccurately neglected inductive effects. Kahng and Muddu [2] proposed a π-model for distributed *RLC* interconnects to estimate the driving point admittance at the output of a CMOS gate. A good and simple approximation of an interconnect line is obtained with the π-model, achieving better accuracy in estimating output waveform and delay calculations. The π-model becomes more accurate as the resistance, capacitance and inductance of the distributed *RLC* line increases. An attempt to model the interconnect line by distributed *RLC* line was made in [3-10], however the driving CMOS gate was replaced by a simple resistor. In estimating the effect of inductance, when an equivalent linear resistor is used to model the nonlinear CMOS transistors, leads to discrepancy in results. This linearization of the transistors results in an overestimation of the inductance effects. This behavior can be understood by noting that a transistor in a CMOS gate operates partially in the linear region and partially in the saturation region during switching. In the linear region, the transistor can be accurately approximated by a resistor. However, in the saturation region, the transistor is more accurately modeled as a current source with a parallel high resistance. The Thevenin equivalent of this circuit is a voltage source with a high resistance in series. This high resistance in series with an interconnect line overrides the series resistance and inductance of the line. Thus, the interconnect appears

Indian Institute of Technology-Roorkee, Roorkee-247667, Uttaranchal, India
Mody Institute of Technology and Science-Sikar, Rajasthan, India, ** Senior Member IEEE

COMPARISION OF COMPRESSION TECHNIQUES FOR FPGA CONFIGURATION BIT STREAM

Komala Soares[1]

Abstract

Field Programmable Gate Arrays (FPGAs) are a promising technology for developing high performance embedded systems the density and performance have drastically improved over the past few years. Consequently, the size of configuration bit streams has also increased considerably. The time it takes to reconfigure Field Programmable Gate Arrays can be a significant overhead for reconfigurable computing. This overhead limits the speedups possible in this exciting new paradigm. In order to deal with this overhead, and increase the compute power of reconfigurable systems, it is important to develop hardware and software systems to reduce and eliminate this delay. This paper brings out the study of compression techniques for all versions of Field Programmable Gate Array configurations that can significantly reduce this overhead. Online and offline compression techniques and the decompression hardware are discussed and compared with practical results. The compression techniques include Huffman coding, the arithmetic coding, LZ coding, the Read back algorithm, the frame recording technique, and the built-in wild card approach

Keywords: ***compression techniques, configuration bits, FPGA.***

1. Introduction

Field Programmable Gate Arrays (FPGAs) are often used as powerful custom hardware for application that requires high-speed computation. One of the major benefits provided by FPGAs is the ability to reconfigure during execution. For the systems in which reconfiguration was done infrequently, the time to reconfigure was of little concern. As more and more applications involve run time reconfiguration, fast reconfiguration of FPGAs becomes an important issue. It is obvious that the reduction in the number of cycles wasted in reconfiguration can generate significant improvement in performance.
Many methods are studied that can reduce the overhead. The compression of the configuration streams such that the total numbers of write operations to load a configuration can be reduced.

Configuration compression using wild card registers achieves good compression for Xilinx 6200 FPGA, but cannot be applied for new generation FPGA with

[1]Contact information: Asst. Professor, Dept. of Electronics and Telecomm, PCC E, Verna, Goa 403722, komala@pcce.org

Simulation of Silicon Nanowire Field Effect Transistors, Carbon Nano Tube Field Effect Transistors and Comparison with Double Gate di-electric silicon MOSFET

E.N.Ganesh[1], P.K.Singh[2], Lal Kishore[3]

Abstract

This paper discuss about simulation of silicon nanowire field effect transistors, Carbon nano tube field effect transistors and comparison with double gate di-electric silicon MosFET. When we improve GCP from 0.88 to 0.9 much improved performance in the device metrics of silicon nanowire FET can be obtained. Hence higher gate control needed for silicon Nanowire transistors. CNTFET of 77k and 300k temperature are simulated. We compared with double gate di-electric Silicon MoSFET. it is shown that CNTFET has higher switching speed, carrier injection velocity, low subthreshod swing, lesser Ion and Ioff currents, but moderate voltage gain. Silicon Nanowire has high voltage gain than silicon MOSFET.

1 Introduction

The scaling of MOSFET below 10nm with efficient gate control is needed, so silicon nanowires nowadays with multi gate and gate all around trasistor being explored{1-6]It is proved by saito etal that silicon parallel nanowire transistors exhibits short channel effects better than single and double MOSFET. So considerable research activities in studying and simulating nanodevices like Single Nanowire transitors and Carbon Nanotube transistors are being considered.

1.1 Single Nanowire transistors

To get decreased subthreshold swing and low leakage current slicon nanoscale MOSFET, silicon nanowire FET and CNTFET are simulated and compared. Silicon nanowires FET (SNWFET) gives higher mobility than nanoscale MOSFET. [7]. Silicon nanowire transistors (SNWTs) have attracted broad attention as a promising device structure for future integrated circuits. Figure 1 shows the schematic structure of silicon nano wire from[10]

Figure 1 schematic structure of the simulated silicon nanowire transistors

1.2 Carbon nanotube FET

The carbon nanotube (CNT) is a hollow tube composed of carbon atoms. Its diameter averages tens of nanometers (10-9 meters) and its length can vary from nanometers to centimeters (10-2 meters). Since their discovery in 1991, carbon nanotubes have been widely experimented with, and analyzed, for their potential

enganesh50@rediffmail.com

A NOVEL ALGORITHM FOR FAULT DIAGNOSIS IN ANALOG CIRCUITS USING SMALL CHANGE SENSITIVITY COMPUTATION

Vishal Gupta[1], Design Engineer
S.C. Bose[2], Senior Scientist
Dinesh Jain[3], Design Engineer

Abstract

In this paper, we propose a novel algorithm to detect and predict faults in the given MOS based analog circuit. The algorithm is based on the concept of differential sensitivity and is able to estimate accurately the value and location of fault. The concept of testable frequencies has been introduced which help in minimizing the computational resource usage by limiting the analysis to a smaller band of frequencies thereby leading to an effective and efficient solution for fault-analysis problem. The algorithm has been tested for single and double fault cases for an Op-Amp but can be extended to multiple fault cases in complex analog circuit as well.

Keywords: *differential sensitivity, testable frequency, sensitivity computation*

1. Introduction

Analog integrated circuits, in addition to digital and RF circuits, are an integral part of SoCs. While the testing and testability of digital circuits is mature and established, there remain considerable difficulties in testing of analog integrated circuits [3,10]. There are several models [4-9,14-16] proposed in literature but the detection of a faulty circuit does not throw any light on the cause of the fault. There have been attempts to diagnose faults in analog system [3,7,11] but these efforts concentrated on the passive components (resistors and capacitors) with the assumption that active components like Op-Amps were fault free. In earlier work [2], authors have used 'IDDQ like' method to identify the cause of the fault in a CMOS op-amp and depending upon the value of the current drawn from supply they were able to club possible faults into certain groups but failed to identify them within the group. The basic concept of the current work is based on sensitivity computation. Sensitivity curves and their properties were explored by the authors in one of their previous works [1]. This work extends previous attempts and proposes an algorithm to solve the fault-analysis problem.
This work has been divided into six sections. Section 2 gives a brief overview of the principle of testability analysis and its usage in the current work. Section 3

[1] ST Microelectronics Pvt Ltd, Greater Noida, vishal.gupta@st.com
[2] CEERI, Pilani, subash@ceeri.ernet.in
[3] Analog Devices, Bangalore, dinesh.jain@analog.com

AN IMPROVED DIRECT INJECTION READOUT STRUCTURE FOR IR FPA

G. Rajahari[+], Anil K. Saini[*], S. C. Bose[*] and Chandra Shekhar[*]

Abstract

In this paper, an improved Direct Injection (DI) current readout structure for 8X8 infrared (IR) focal-plane-array (FPA) is presented. In-pixel switch current integration technique and cascode bias transistor have been used to control the integration time and to maintain stable detector bias voltage respectively. An in-pixel sample-hold switch is used to allow maximum possible frame rate and integration time duty cycle. This read-out integrated circuit (ROIC) architecture for the IR FPA is realized using improved DI circuit having a pixel-size of 48µm X 52µm that can be operated in integration-while-read (IWR) and integration-then-read (ITR) mode. The physical design of the 8X8 array ROIC circuit has been done in SCLs 1.2µm single-poly-double-metal n-well CMOS technology and sent for fabrication to SCL under India Chip program.

Key Words *Direct Injection, FPA, ROIC*

Introduction

In the design of infrared (IR) focal plane array (FPA), high resolution has become a common requirement in many applications. High resolution requires large pixel array and consequently smaller pixel size to reduce the overall area of the pixel array. So far, a large number of pixel architectures have been reported in the literature. Direct Injection (DI) circuit, and Gate-Modulation Input (GMI) circuit [1], [2] requires small area but does not provide good performance in terms of injection efficiency and detector bias stability. Both Buffered Direct Injection (BDI) and Capacitive Trans-Impedance Amplifier (CTIA) [2] circuit have in-pixel integration capacitor and each provides better performance (compared to DI and GMI circuit) in terms of injection efficiency and detector bias stability with the use of an in-pixel op-amp. This would increase the pixel area and the performance of the pixel is obviously limited by the performance of op-amp. Buffered gate modulation integration (BGMI) [3] and switched current integration (SCI) [2] has off pixel integration capacitor but has op-amp inside the pixel, which would contribute to the pixel area and also

[+] Project Assistant at CEERI, Pilani. Currently at Sasken as Design Engineer
[*] Scientists at CEERI, Pilani

ARCHITECTURAL DESIGN AND IMPLEMENTATION OF A PC BASED ULTRASOUND IMAGING SYSTEM

Bodhisatwa Mazumdar[1], Aman Mediratta, Joydeep Bhattacharyya, Swapna Banerjee

Abstract

This paper presents the architectural design and implementation of hardware blocks of ultrasound imaging system. The system blocks include an analog front-end, a few digital signal processing hardware units. The digital signal processing units are implemented using Xilinx FPGAs, due to the need for both real time operation and further reconfigurability, if required. Extensive parallelism and pipelining have been exploited while mapping the algorithms into VLSI. The blocks described below are being implemented on different FPGA chips for optimum resource utilization as well as considering the speed-up issues.

Keywords: *Ultrasound, beamforming, apodization, scan conversion, CORDIC.*

1. Introduction

Over the last two decades, ultrasound has become a key player in medical diagnostics. Being a safe, painless and noninvasive method and also because of the absence of any ionizing radiation, it has established itself as probably the most useful among all imaging methods in fields like obstetrics. The anatomy can be studied from gray-scale B-mode images, where the reflectivity and scattering of the tissues are displayed (Shoup and Hart, 1988).

Real time medical imaging needs low power, high-speed operation which can be achieved by extensive parallelism and pipelining, the partitioning of the tasks being a function of the requirement as well as the inherent regularity and modularity of the algorithms.

The proposed system is fully PC compatible. Most of the data processing is taken care of by dedicated hardware, relieving the CPU from heavy computational load. This also supports real time processing, display and storage of data, all at the same time. It is possible to obtain contrast enhanced and noise cleaned still images also. However, the machine has dedicated hardware for image compression and coding. Hence, one can have storage of compressed video frames, as and when dictated by the user. The data processing and the storage blocks if implemented on PC will have severely degraded speedup and also the portability of such a system will be restricted.

[1] Contact information: Bodhisatwa Mazumdar, IIT Kharagpur, bm.iitkgp@gmail.com

DESIGN OF AN EFFICIENT LOW POWER AES ENGINE FOR ZIGBEE SYSTEMS

Ninad B Kothari[1], T.S.B. Sudarshan[2], Shipra Bhal[1], Tejesh.E.C[1], S. Gururnarayanan[3]

Abstract

This paper presents an AES engine especially designed for a Zigbee SoC solution. The proposed architecture has not only been designed to meet the power requirements of Zigbee but also the other protocol specific aspects like dynamic key changing and the decision making capability of whether to encrypt data or not. Some of the key hardware blocks like the State Matrix, Mix Columns, Key Generation and Sub Bytes have been custom designed for low power. Although the proposed architecture has been designed for Zigbee, it can be interfaced with other General Purpose Processors with some adequate Glue logic. The proposed architecture has been compared with existing architectures to demonstrate that it is best suited for a Zigbee SoC solution.

1. Introduction

Intelligent self-forming and self-maintaining wireless networks is a dream fast becoming reality. Zigbee is one of the strongest contenders among the slew of technologies vying for large market space. The major assets of Zigbee being, its open standard, simplicity of protocol,, and considerable industrial support, it is fast gaining popularity among both chip designers and vendors. The Zigbee Alliance has stressed on high levels of security from its basic inception. AES being one of the robust security standards, it has been chosen to be the security algorithm in Zigbee.The three main focus areas in Zigbee are low power, longer battery life and lesser system complexity compared to other existing wireless standards. Zigbee derives its low power capability by not only reducing the data rate but also the clever use of its network resources. Zigbee is an open standard whose PHY and MAC layers are defined b^{2}y the IEEE 802.15.4 [1] and the NWK and APP layers are defined by the alliance [2]. Zigbee caters to the mesh type, star type and tree topologies. Most Zigbee applications are targeted towards the low data rate groups like unattended wireless systems in homes, offices and factories. The compromise is, fairly modest bit rates –a maximum of 250 kbps, and a very small node-to-node spread. The ranges are generally about 10m. The Mesh networking makes up for the limited power of each individual node by leveraging the ability to relay data through nearby cooperating nodes [3], [4] thus increasing, the reach of each node.

Zigbee defines a 128-bit block cipher, AES [2], [5] (Advanced Encryption Standard) as the security system for the protocol. The protocol defines a set of

[1] Student, Electrical & Electronics Group, BITS, Pilani
[2] Assistant Professor, Computer Science Group, BITS, Pilani.
[3] Professor, Electronics & Instrumentation Group, BITS, Pilani

ON THE QUALITY OF TRANSITION FAULT TESTS

Jais Abraham[1], Sandeep Jain[2]

Abstract

Transition fault model based test patterns are increasingly being used on high-speed designs to ensure that they do not contain defects which would prevent them from working at their rated speeds. This delay fault model helps to cover the gross delay defects existing in the circuit more efficiently than other known delay fault model. However, the absence of timing information of design nodes during the generation of these patterns is an inherent limitation of this fault model. In this paper, we propose various techniques by which the timing information of the nodes in the design can be exploited to improve the quality of transition fault patterns and to reduce their test application time. A model to compute the quality of transition fault pattern sets is also described which provides a better metric of the delay fault detection capabilities of transition fault patterns compared to their coverage.

Keywords : Delay Fault Testing, Quality of Transition Fault Tests

1. Introduction

The advent of deep submicron (DSM) technologies has opened up opportunities for the creation of designs working at gigahertz or near gigahertz speeds. However, these technologies are also more prone to process variations and random defects and hence more complex tests have to be created to ensure the quality of the manufactured devices [1]. Stuck-at tests are no longer considered sufficient for the detection of defects on these devices. Increasing speeds and technology scaling has made these devices increasingly prone to delay defects. These defects prevent the devices from working at their designed frequency.

Multiple fault models have been proposed to detect delay faults. The most popular among them include the transition fault model and the path delay fault model [2,3]. Transition fault tests are targeted for the detection of large delay defects on nodes, whereas path delay tests target finer defects which can occur along paths. Both the delay fault models require the generation of a two

[1] Contact Information: InnoDes Solutions Pvt. Ltd., Bangalore.
jais.abraham@innodes.co.in
[2] Contact Information: Texas Instruments (India) Pvt. Ltd., Bangalore.
jainsandeep@ti.com

SPECTRAL CHARACTERIZATION OF FUNCTIONAL VECTORS FOR GATE-LEVEL FAULT COVERAGE TESTS

Nitin Yogi[1] and Vishwani D. Agrawal[1]

Abstract

Vector sequences generated from functional description of digital circuits exercise a sufficient set of key or critical operations and are used for verification of pre-synthesis architecture and post-synthesis logic design. We analyze these vectors using Hadamard matrices and determine the prominent or essential Walsh spectral components and the low intensity noise-like components. This implementation-independent spectral information is then used to generate fault coverage vector sequences for gate-level non-scan implementations by making use of Hadamard matrix again and by randomly perturbing the Walsh spectra in which the essential components are left unperturbed. At the gate-level, a fault simulator is used to compact the vector sequences. We give results for three non-scan ISCAS'89 and one ITC'99 benchmarks for which functional descriptions were available. Our results show that the spectral vectors are comparable in fault coverage and test length to gate-level sequential ATPG.

1. Introduction

Verification of a digital system checks the functional correctness, which is essential before proceeding with low-level implementation and manufacture. Verification vectors are created from the knowledge of the input-output behavior and exercise all or most functions with selected critical data patterns. These vectors are used for simulation of the architecture-level, register-transfer level (RTL), and gate-level designs. Such vectors are also found to be useful in detection of several kinds of manufacturing defects such as timing faults. However, they have not been used in manufacturing test because of a usually low gate-level stuck-at fault coverage and large test data volume. Therefore, the problem of finding a small subset of functional vectors with high fault coverage is of interest.

We develop a new spectral method to generate vectors that resemble, though they are not the same as, functional vectors. Analysis shows that the temporal behavior of a functional vector sequence is largely described by a digital spectrum of Walsh functions. Besides, recognizable Walsh functions a functional sequence also contains random behavior. Using these two characteristics, we generate vector sequences for gate-level fault coverage. Only a gate-level fault simulator is used; no ATPG program is required.

2. Background

Background work related to our research has been in two directions, namely, behavior or RTL test generation, and spectral test generation.

[1] Auburn University, Dept. of ECE, 200 Broun Hall, Auburn University, AL 36849, USA; Email: yoginit@auburn.edu, vagrawal@eng.auburn.edu.

CROSS TALK AWARE MULTI-OBJECTIVE OPTIMAL ROUTING FOR ISLAND-STYLE FPGAs

Rajesh Tiwari[1] **V. Sahula**[2]

Abstract

Field programmable gate arrays (FPGAs) have become imperative for implementing large digital circuits in customized VLSI circuits. A key component in the design of an FPGA is its routing architecture, which comprises of the wiring segments and routing switches that interconnect the FPGA's logic blocks. In order to obtain optimal routing solution in a reasonable amount of time, evolutionary approaches are employed, which provide better quality solutions in shorter run times compared to other approximate algorithms. Evolutionary approaches perform even better when optimization of multiple objectives is considered by virtue of their population-based exploration strategy. This paper illustrates the optimization of the delay and cross talk both for FPGA routing using non-dominated-sorting-genetic-algorithm (NSGA) methodology as proposed by N. Srinivas and K. Deb (1994), formulated as multiple objective optimization problem. The proposed global router accepts placed-netlist as input; divides connections into two-point connections and then routes each of them separately. The routing is optimal for both the delay and cross-talk for a connection.

1. Introduction

Nowadays, Field-Programmable Gate Arrays (FPGAs) are being widely accepted as means of implementing large digital circuits in a customized VLSI chip. *Array-based* architecture is one of the most significant types among a large number of commercially available styles of FPGAs, It consists of rows and columns of logic blocks with horizontal routing channels between the rows and vertical channels separating the columns.

The traditional routing strategy is a two-stage approach, in which global routing is followed by detailed routing. There are three main concerns of the present work- (i) Multiple Objectives, (ii) Evolutionary algorithm approach (i.e. Genetic algorithm), and (iii) Routing for FPGAs. One of the most important aspects of our work is multi-objective optimization, where we consider two objectives crosstalk and delay both of which have to be minimized for a connection. Genetic algorithm (GA) works on a collection of several alternative solutions to a given problem. Each solution in the population is called a string or chromosome. GA, which is a probabilistic approach, searches for the population of points instead of single point. Our approach borrows the genetic operators' formulation from C. W. Ahn and R. S. Ramakrishna (2002). The crossover operation exchanges partial chromosomes (partial routes) at positionally independent crossing sites and the mutation operation maintains the genetic diversity of the population. The algorithm can cure all the infeasible solution

[1] Design Engineer, Texas Instruments, Bangalore. rktiwari@ti.com
[2] Reader (Assoc. Prof.), Department of ECE, NIT Jaipur. sahula@ieee.org

ROBUST POWER DELIVERY FOR SUB-100NM INTEGRATED CIRCUITS

Thenappan Meyyappan[1], V Visvanathan[2], S K Nandy[3]

Abstract

Modern day integrated circuits are moving towards higher frequencies, higher power consumption and reduced supply voltages. The relentless march of technology scaling has resulted in faster devices enabling high performance systems. At the same time due to the increasing density, they draw higher current and dissipate more power. The task of designing a power delivery network with minimal noise is becoming more and more complex. In this tutorial, we look at aspects of design and analysis of on-chip power/ground network. Techniques to estimate the required decap and allocate them at appropriate design stage are discussed. Variations in the supply voltage causes uncertainty in gate delays and impacts timing. The limitations of the current timing analysis techniques to comprehend these issues is highlighted. Vectorless analysis techniques that integrate both power supply noise analysis and its impact on timing are discussed. . Finally we briefly touch upon the inductance effects in a power distribution network and design techniques to counter them.

1. Introduction

With the increasing complexity of Integrated Circuits (ICs), the design of a robust power distribution network has become extremely complex and demanding. Modern high performance processors dissipate power upwards of 100 Watts. At an operating voltage of 1V, the impedance of the power distribution network has to be less than 0.5 mΩ for the voltage drop to be within 5% of the supply. Large currents of the order of 100A flow through the power distribution network and faster switching devices result in sharp transient current. Large currents contribute to high ohmic drop and transient current causes large inductive drop in the supply voltage. Power supply noise is projected to become a serious issue in achieving design closure starting 2007 [ITRS (2005)].

The advent of sub-100nm process technologies has brought about various challenges in power/ground integrity and emphasizes the need for robust power delivery mechanism to safeguard the chips against failure.

- Due to smaller device area and increased die size, it is possible to pack more transistors in a chip than before. There is an increase in the total power demand and coupled with voltage scaling, implies large currents through the power distribution network.

[1] Texas Instruments, Bangalore. thens@ti.com
[2] Texas Instruments, Bangalore. vish@ti.com
[3] CAD Lab, Supercomputer Education and Research Center, Indian Institute of Science, Bangalore. nandy@cadl.iisc.ernet.in

INTEGRATED STABILITY ANALYSIS METHODS FOR HYBRID MICROSYSTEMS

Jairam S[1] Navakanta Bhat[2]

Abstract

Traditional stability analysis methods for systems have been applied with a control system perspective. SoCs based on hybrid microsystems are a case where these methods have not been well defined. In this paper we propose two different methods of stability analysis for such problems. Methods for circuit stability have been explored and extended into control systems based methods for hybrid components. A mechanical beam capacitance structure and a thermal domain based hybrid system have been analysed with the proposed methods.

1. Introduction

The most popular ways of analysing systems for their stability are the control-systems based methods [1]. However these methods assume systems to be represented in their respective time/frequency domain formats. In other words they need to be well-posed. State space based methods are one of the most elegant and simple representations. The present day systems however include many non-linear sub-sets where these control system based methods may not be directly applicable. These components are analysed through numerical or semi-analytical methods. But when one has to solve for the complete solution and look at its behaviour, these solution subsets cannot be separated. As a result need is felt for less intensive and more intuitive methods to solve these kinds of problems. Methods like FEM/BEM for detailed analysis are available for respective energy domains, but simple visualisations of solution for the integrated problem can provide much deeper insight into the working of systems. Such requirements are becoming very important for MEMS based SoCs.

We divide such problems into two classes' viz. standard class and heterogeneous class. Standard class includes routine control kind of problems where there exist multiple ways for analyses. Nyquist, Bode plots, Route-Locus, Routh-Hurwitz etc are some of the most popular methods that solve the problem in different ways. Frequency representation is preferred for all the standard class problems. However the heterogeneous class cannot be grouped into one category alone. As the name suggests, the nature of the problem can be very diverse. Examples can be mechanical structures (beams), fluidics (pumps), optics (micro mirrors), thermal (heat sensors) etc. Slowly as systems turn towards multiple energy domains, early top level analysis becomes more and more important. Analysis methods for these classes of problems can be as varied

[1] SDTC Texas Instruments. sjairam@ti.com
[2] ECE Indian Institute of Science. navakant@ece.iisc.ernet.in

DESIGN AND ANALYSIS OF ROBUST CLOCK TREES

Madhusudan Rao, Jagdish Rao, V. Visvanathan, Udayakumar H

Abstract

The primary concern of clock distribution has been to minimize skew. With increasing die sizes in very small feature processes and frequencies approaching GHz, skew changes of the order of tens of picoseconds could impact performance and yield. The delay degradations are induced by the process variations impacting device and interconnect parameters. Present CAD solutions which implement clock distribution in standard cell SoCs do not necessarily comprehend process-induced variation. In this paper, we present design practices and solutions to enhance robustness to variations. We also develop methods to measure the degree of robustness of clock trees in the context of corner-case analyses.

Keywords*: Clock distribution, process variation, robustness to variation, Clock Tree Synthesis, clock skew*

1. Introduction

As clock frequencies approach the GHz range, variations of tens of picoseconds could degrade the performance of synchronous systems. Such delay degradations are common in present-day feature sizes (90nm, 65nm) and beyond, coming from manufacturing process changes with respect to the process specification. These variations besides having impact on yield at the targeted frequency of operation can have disastrous effect on circuit reliability. On the other hand, if the variations are not understood, highly pessimistic design margins will be required to guarantee product performance specs while achieving a profitable yield. Clock skew changes have the single biggest impact in synchronous systems. Today's CAD solutions for clock distribution in standard cell designs, do not necessarily comprehend these parametric changes. In this paper, we present sources of variation and impact on clock skew in the next section. In Section 3, we briefly survey clock distribution approaches. In section 4, design practices and guidelines to improve robustness in clock trees are explained. Section 5 introduces metrics to analyze and compare clock trees for robustness.

2. Sources of Variation and Impact on Clock Skew

The effect of variation on circuit performance can be from two distinct source sets [1, 12]: ***Environmental*** and ***physical***.

- *Environmental sources* include temperature changes and power supply variation and noise. The temperature gradients are due to activity or inactivity in circuits. The impact of temperature changes is becoming more

Abstract:

Color is all around us. It is a sensation that adds excitement and emotion to our lives. Everything from the clothes we wear, to the pictures we paint revolves around color. Without color, the world would be a much less beautiful place. But this is what is experienced by blind or color blind people. This project is an attempt to help these people identify colors around them.
Color data is obtained by balancing the relative intensities of RGB primaries. This device is able to identify a number of colors. The output of the device is sound.

1. Introduction:

Over time, a number of devices have been developed for the visually impaired people to identify colors. These devices help the visually impaired people to enjoy the colorful world to some extent. These devices make them self efficient in situations where interpretation of colors is crucial, such as interpreting the traffic lights. This project explains about one such device that serves this purpose.

Light is a form of electromagnetic radiation. This radiation contains radio waves, visible and X-rays. Electromagnetic radiation is a spectrum of radiation extending beyond the visible radiation to include at one end radio waves and at the other end gamma rays. The visible light region occupies a very small portion of the electromagnetic spectrum. It is the range of wavelengths that the eye responds to. Although radiations of longer or shorter wavelengths are present, the human eye is not capable of responding to it.

A color's spectral signature may be identified by noting its wavelength. We sense the waves as color, violet being the shortest wavelength and red the longest. The range of wavelengths (400 - 700 nm) of visible light is centrally located in the electromagnetic spectrum.

Light is also considered as a stream of minute packets of energy-photons - which create a pulsating electromagnetic disturbance. A single photon of one color differs from a photon of another color only by its energy. Visible light is composed of photons in the energy range of around 2 to 3 eV. As the energy of the light increases, the wavelength decreases. The intensity or brightness of the color is defined by the flux, or number of photons passing through a unit area in a unit time; i.e., number of photons per cm^2 per sec.

2. The Color of Objects:

Color is produced by the absorption of selected wavelengths of light by an object. Objects can be thought of as absorbing all colors except the colors of their appearance which are reflected as illustrated in Fig. 1. A blue object illuminated by white light absorbs most of the wavelengths except those corresponding to blue light. These blue wavelengths are reflected by the object.

ABSTRACT:

We propose a method of eigen faces to represent an emotional state of an animated agent, onto muscle contraction values for the appropriate facial expression. The aim is to provide a software simulation of the neutral human face in two dimension(2-D). Attention has been focused on the face as an important means of non-verbal communication. The interactive composition and modification of human facial parts have been identified as being of particular interest, this uses eigen vectors that is defined based on the study of minimal facial actions and is correlated to muscle actions. The analysis includes the generation of eigen matrix for a neutral cartoonic face and a subsequent generation of new variables, using an ideal data matrix as a point of departure in such a way that these variables can express more structurally the variability of the initial matrix.

1. INTRODUCTION:

The face is a rich source of information about human behavior. Facial displays indicate emotion, pain, brain function and pathology, and regulate social behavior. In daily life, expressions occur relatively infrequently, and emotion more often is communicated by change in one or two discrete features, such as tightening the lips in anger. Facial muscles correspond for these facial expressions. The facial muscles are like elastic sheets that are stretched in layers over the cranium, facial bones. These are the muscles of facial expression, acting singly and in combination.

There are 21 muscles which corresponds for facial expressions[2],which are:-
[inner/outer frontalis] [corrugator] [procerus] [depressor supercilli] [inner/outer orbicularis oculi] [nasalis] [depressor_septi] [levator_labii] [buccinator] [caninus] [risorius] [zygomatic_major] [zygomatic_minor] [depressor_labii] [orbicularis_oris] [masseter] [triangularis] [mentalis] [platysma]

Their use can be listed as below....

Frontalis: this muscle raises and lowers the eyebrows and moves during speech
Curragator: this muscle assist in brow motion during emotions (anger, fear, sadness, ...)
Levator Palpebrae: this muscle raises and lowers the eyelids
Orbicularis Oculi: this muscle is used for eye movements

Seven muscles work together to move the lower face with the mouth and jaw:

- **Orbicularis Oris:** this muscle tightens the lips into a pursed position
- **Zygomatic Major:** this muscle pulls the face into a wide grin
- **Levator Labii Superiors:** this muscle raises the upper lip and the nose

Abstract:

Agriculture has always been India's most important economic sector. Higher agricultural growth leads to rural prosperity and that triggers high economic growth. Agriculture is the starting point for India to emerge as an economic super power. Hereby we present a method to improve the yield by means of changing the **square** sowing pattern to **hexagonal** one. The net improvement in the usage of land by such a method is almost **13.5%** as compared to the conventional method. The net crop density is increased in the hexagonal pattern, this results in **reduced weed growth** which in turn helps efficient water and soil management. In this pattern as the continuous gap between plants is very less, unlike square pattern, this resists **erosion** of soil by wind and water. The usage of sunlight in this pattern is found to be efficient. Further, we decide upon the average length of the plants to be plotted in the field and talk of the orientations of the field so that the shadow due to one plant does not adversely affect others. Finally we will realize that the price we need to pay for increased yield is too less, just matter of changing sowing pattern.

1. Introduction:

In order to break into a high trajectory growth rate on a sustained basis we have to start with agriculture. Higher agricultural growth leads to rural prosperity which, in turn, leads to more buying power, and that triggers high industrial growth. Thus, agriculture is our biggest asset. In the mid-1990s, it provided approximately one-third GDP and employs roughly two-thirds of the population. But, in contrast, the capital formation in Indian agriculture is declining from year to year down from 17 per cent in 1980 to 9 per cent now. So agriculture in India has been increasingly neglected.. Thus need of the hour is to use this available land efficiently which would lead to our over all progress.

We discuss a new pattern of sowing seeds in a field other than the conventional method which will lead to efficient usage of land. Square pattern is the most commonly used seed sowing pattern. In this case rows and columns are formed to have squares in between and the plants are plotted at center of each square. If we consider that a plant occupies a circular space of radius 'r', radius being dependent on the type of plant, then for each square 22% of land is wasted. Now we go in for Hexagonal pattern of sowing seeds of same plant. In this case only 9% of land is wasted and the yield is increased to almost 14% as compared to that in Square pattern.

There are many factors that decide the yield of the crops such as Sunlight, Weeds, Soil erosion, Fertility and nutrient content of the soil, Intercropping etc. One by one we discuss the effects of each factor on plants in Square and Hexagonal pattern and talk of advantages of the latter. At the end we will find out that the price we pay for increased yield is too less and now its high time that we should change the trend of seed sowing pattern from Square to Hexagonal one so that it results in healthy and high yield leading to efficient farming and indeed progress of our country.

Abstract

SuDoku is a popular puzzle that can be very addicting. It starts with 9 x 9 grid that has some digits placed in particular cells. Fill in the grid so that every row, every column, and every 3 x 3 box contains the digits 1 through 9.Among the three algorithms used, the first is based on the concepts of set theory using operations like union and complement. This is based on the principle that, no row, no column and no box can contain repeated numbers. First method gives the probable numbers to be entered in the blank cell. The second algorithm seeks the help of subsets. The third algorithm, which applies frequency determination of each number is particularly useful in difficult puzzles. The presence of a singleton confirms the number at that place. Simple C programming is used to implement the algorithms. The hardware part involves realization of first algorithm. Basic gates, decoder and registers are used for its implementation. With a bit of complexity involved, these sudoku puzzles can be downloaded on cell phones thus increasing their popularity.

1. Introduction:

Have you heard anything about the popular addicting play SuDoku? If not, open any newspaper. It is a fun puzzle dealing with numbers, but it is not Mathematics! This puzzle involves simple reasoning and player is not bound to use complex calculations. This is a simple number game of filling some digits in a grid of cells. The attraction of the puzzle is that the completion rules are simple, yet the line of reasoning required to reach the completion may be complex.

Our project involves simple C program which would check for the solution given as the input entered by the player, in case the solution is incorrect it generates the solution and displays it. We use the memory bank which has stored SuDoku puzzles which has to be solved by the player.

1.1. History:

Leonard Euler, Swiss mathematician in 1783 invented Latin squares (N*N grids) which had all numbers from 1 to N appearing only once in each row and column .Inspired by this Howard Garns a retired architect and freelance puzzle constructor designed the puzzle in 1979.The puzzle was introduced in Japan by Nikoli in the paper Monthly Nikolist in April 1984 as 'Suji wa dokushin ni kagi' which can be translated as 'the numbers must be single' or 'the numbers must occur only once.' The puzzle was named by Kaji Maki, the president of Nikoli. At a later date, the name was abbreviated to Sudoku. The name 数独 or Sudoku comes from Japan and consists of the Japanese characters Su (meaning number) and Doku (meaning single) but the puzzle itself originates from Switzerland and then travels to Japan by way of America.

In 1986 some important improvements were added, mainly by making symmetrical patterns and reducing the number of given clues, Sudoku became one of the best selling puzzles.

ABSTRACT:

Sleep is a fundamental activity that consumes one-third of our lifetimes. The earliest hints that sleep was a changing state came with studies showing that blood pressure, pulse rate, and other body functions in humans rise and fall in a pattern during sleep. When prematurely awoken from sleep we tend to feel groggy .We have designed an alarm clock that wakes you up naturally. Before you go to bed, an optical sensor has to be placed at the finger tip and the alarm clock is set(for example 6 am).The sensor consists of a light source and photo detector, light is shown through the tissues and variation in blood volume alters the amount of light falling on the detector. This input from the sensor is sent to the main circuit which measures the pulse rate and hence the stage of sleep. If you are not in a shallow stage of sleep, at around 5.30 am it gives you a buffer to naturally progress into shallow stage so you wake up refreshed. This is done by gradually increasing the light intensity of the room. This turns out to be better than the conventional alarms which wake you up with a jarring sound.

1. INTRODUCTION:

Much of what is known about sleep stems from the groundbreaking 1953 discovery of rapid eye movement (REM) sleep. This is an active period of sleep marked in humans by intense activity in the brain and rapid bursts of eye movements. When we switch into REM sleep, our breathing becomes more rapid, irregular, and shallow, our eyes jerk rapidly in various directions, and our limb muscles become temporarily paralyzed. Our pulse rate increases and blood pressure rises.

Scientists divided non-REM sleep into four stages, accounting for about 75 percent of total sleep. In each stage, brain waves become progressively larger and slower, and sleep becomes deeper. After reaching stage 4, the deepest period, the pattern reverses, and sleep becomes progressively lighter until REM sleep, the most active period, occurs. This cycle typically occurs about once every 90 minutes in humans.

Studies show that the length of sleep is not what causes us to be refreshed upon waking. The key factor is the number of complete sleep cycles we enjoy. Each sleep cycle contains five distinct phases, which exhibit different brain-wave patterns. For our purposes, it suffices to say that one sleep cycle lasts an average of 90 minutes: 65 minutes of normal, or non-REM (rapid eye movement), sleep; 20 minutes of REM sleep (in which we dream); and a final 5 minutes of non-REM sleep. The REM sleep phases are shorter during earlier cycles (less than 20 minutes) and longer during later ones (more than 20 minutes). If we were to sleep completely naturally, with no alarm clocks or other sleep disturbances, we would wake up, on the average, after a multiple of 90 minutes-for example, after 4 1/2 hours, 6 hours, 7 1/2 hours, or 9 hours, but not after 7 or 8 hours, which are not multiples of 90 minutes. In the period between cycles we are not actually sleeping: it is a transition zone from which, if we are