THE GROWING SEMICONDUCTOR ZOO: ASICS, STRUCTURED ARRAYS, FPGA, PROCESSOR ARRAYS, PLATFORMS AND OTHER ANIMALIA

Dr. Raul Camposano[1]

ASICs (and ASSPs) have been a formidable driving force for the semiconductor industry. In particular, ASIC design has been the major consumer of EDA tools and design technology in the past. However, ASIC design starts have declined lately and many voices speak of fundamental change beyond the current downturn, predicting even the extinction of ASIC design altogether. One of the main culprits is certainly raising NRE costs: it costs approximately $10M to design an ASIC in 130nm technology, and that cost will just increase as geometries get smaller and design gets more technically challenging. Other vectors making ASIC life difficult include cost of respins, lack of flexibility (compared to programmable solutions) and the demanding task of designing them, resulting in increased time to results.

These problems are being addressed by a variety of alternative silicon "fabrics": structured arrays, FPGAs, processor arrays and "platforms" are all trying to fill the void left by the slowing of ASIC production. The reality is that none has so far proven to be a complete solution from either an economic sense or a performance/application perspective. In fact, these alternative solutions might have opened the door wide open for a revival of ASIC design in the form of platforms that intermarry pure ASIC design with one or more of those alternative solutions. This presentation shows the trade-offs among these solutions, compares the tasks of designing in each case, and demonstrates that there is still life left in ASICs. It also looks at several ways of mixing these technologies to add even more variety to the Zoo.

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CONCURRENT ENGINEERING CHALLENGES AND OPPORTUNITIES IN SYSTEM-ON-A-CHIP DESIGNS

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With advances in manufacturing technology, the level of integration and the complexity of system-on-a-chip designs has been growing at a rapid pace. There is an ever increasing need to reduce cycle time for releasing these new, differentiated products to the market. These SoCs typically have one or more programmable processors, and what needs to be delivered to the customer is not just a chip but a complete solution – which involves embedded software and reference design as well. While "spec to tapeout" is the main focus of the SoC design process, the designers need to focus on complete solution delivery and in that context work with the applications team on pre-silicon software validation and with the product engineering team on design-for-test strategy to ensure rapid ramp to production. The "differentiation" of the solution drives aggressive goals in terms of cost (die size + test cost + package cost), performance and power dissipation. These parameters need to be optimized in the solution context which again extends beyond the chip design phase itself.

This talk presents concurrent engineering/co-design challenges and opportunities in the context of chip design done concurrently with other functions such as embedded software development, package design, reference board design etc. The talk also covers challenges and opportunities in concurrent engineering of various phases of the chip design process itself – such as, for example, doing chip level integration concurrently with developing the IP being integrated.

In developing a complete system solution, the SoC design team interfaces with the following functions:

- System/chip architecture definition and validation
- SW apps team developing embedded software
- HW apps team developing reference design
- Packaging
- Fab – design rules, electrical characteristics of transistors and interconnects
- Product Engineering

VLSI Education in India: Towards Excellence, Numbers, and Relevance

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Abstract

VLSI education in India is now on the threshold of a big expansion. Incidentally, this is the silver jubilee year of VLSI education in India. During the quarter century of its existence in the country, it has gained adherents among the faculty of top-rung academic institutions, where it has struck deep roots. Over the last five years or so it has spread to the next rung of academic institutions through concerted government efforts and the increased awareness within these institutions. It is now poised to spread out to the further next rung institutions -- the 'other good institutions of engineering education' -- again through a combination of concerted government efforts and a spreading awareness of the subject in these institutions. The non-university corporate educational/ training ventures are confined to 4-6 month training/diploma courses.

Quality of VLSI education in terms of students becoming well-versed in fundamentals and their applications in problem-solving has been an issue of deep concern among the industrial and government employers of the VLSI-educated. These concerns will become even more acute as further expansion of VLSI education takes place (which it must).

The main problems pertaining to quality have been the lack of adequate faculty-development and the faculty pool to draw on. Even today the hard-core VLSI academic faculty pool is no bigger than 60-70 persons who among themselves rigorously train between 250-300 graduate students and introduce another 1000-1200 under-graduate students to the subject. A TCS-IIT Bombay study-report submitted to the government of India recommends the generation of around 4000 graduate engineers per year in the area of VLSI Design and Embedded System Design in order to meet the Indian and as well as a part of the global demand for such professionals. This calls for a rapid jacking-up of the size of the faculty-pool to 600-700 persons from the current size of 60-70 persons. Building up of such a pool cannot be done unless we harness technology (broadcasting, net-casting, virtual class rooms, e-resource generation/pooling etc.) and with the industry also pitching in -- and not just with financial/hardware-software resources but also with their senior engineers and project-leaders level manpower and technical expertise -- with the full backing of their top-level management.

At the graduate level (and also under-graduate level), project work provides both a specialization and a link to real-life problems for the student. However, the definition and guidance of these projects requires quality faculty in numbers that would take years to build. As a result, academia-industry partnership in this vital area is crucial -- both from the qualitative and quantitative points of view. Major government R&D centres should also shoulder responsibility in this regard.

Slowly academic faculty, as it builds up, should get involved in industrial consulting to build knowledge and personal linkages with industry. Case studies (of large designs), and very specialized innovative designs (not necessarily large) should be regularly shared within the community via specialized lecture-series and seminars.

Faculty training programmes must be conducted very frequently and vigorously by the existing pool of experts in the academia, R&D and industry that the faculty from new colleges can attend. Design walk-throughs must become an integral component in the latter part of these trainings. The architectural issues across hardware-software boundary, their impact on speed, power and cost, the test issues and economic viability issues must be high-lighted through walk-throughs in the design space.

Experience has also shown that a large part of a students learning takes place in the structured laboratory components of their curriculum. Expressing design concepts, ideas and requirements through tools and

Semiconductor Design Outsourcing: Global trends and Indian Perspective

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Abstract

Semiconductor design is becoming a key aspect of product development cycle and customers are keen to see how this phase of the product cycle is optimized. Trends have shown how design outsourcing trends have changed globally and companies in India especially have been taking advantage of this phenomenon. The talk would cover different aspects of semiconductor design outsourcing – drivers for outsourcing, opportunity space, challenges for companies and how we see the trends change in the coming years.

A High Speed Efficient Signed/Unsigned N x N Bit Multiplier Based on Ancient Indian Vedic Mathematics

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Abstract

A fully synthesizable signed/unsigned multiplier based on Urdhva Tiryakbhyam [1] (algorithm of ancient Indian Vedic Mathematics) is presented in this paper. The proposed multiplier is a high speed multiplier and can be implemented for NxN bits. The design implementation is described in both at gate level and high level RTL code (behavioural level) using Verilog Hardware Description Language. The design code is tested using Veriwell Simulator. The code is synthesized in Synopsis FPGA Express using: Xilinx, Family: Spartan Svq300. The implemented design can be easily converted from one technology to another. The present paper relates to the field of math coprocessors in computers and more specifically to improvement in speed and efficiency over signed/unsigned multiplication algorithm implemented in coprocessors. In FPGA implementation it has been found that multiplier based on Vedic Mathematics is faster than array multiplier for both signed and unsigned number.

Keywords: *Vedic Mathematics, Urdhva Tiryakbhyam, Array Multiplier, Signed Vedic Multiplier*

1. Introduction

Hardware multipliers are essential component of all the computer systems, cellular phones and most digital audios / videos etc. The known method of multiplication in a math coprocessors are array multiplication, booth multiplication each with its own limitations. The array multiplier performs the parallel multiplication. The parallel multiplication process is based on the fact that in multiplication partial products can be independently computed in parallel. Array multiplier is a fast way of multiplying two numbers since the delay it takes, is the time for the signals to propagate through the gates that form the multiplication array. However, an array multiplier needs a large no gates and thus they are less economical [2]. In designing of a multiplier, the operation unit such as an arithmetic logic unit (ALU) of a central processing unit (CPU)

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A Low Power Circuit to Generate Neuron Activation Function and its Derivative using Back Gate Effect

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Abstract

A Low power circuit configuration to generate sigmoid neuron activation function (NAF) and its derivative (DNAF) is presented in this paper. Derivative generation is based on introducing asymmetry in a cross-coupled differential pair configuration by biasing the body terminal of one of the driver transistor of each differential pair. The operation of the circuit is presented in the subthreshold region for ultra low power applications using 1.2µm SCL technology. Circuit operates with reduced rail-to-rail power supply of 2V.

1. Introduction

The basic building block of a feedforward neural network (FNN) is a simple processing element called neuron. The model of each neuron in the FNN includes a nonlinear activation function that is monotonically increasing and bounded from above and below. The transfer characteristic of neuron, described by the input/output relationship $y_j = f_j(s_j)$ should be such that $\partial f_j/\partial s_j$ exists and is finite. The symbols y_j and f_j represent output and NAF respectively. Here s_j is the product of input vector and weight vector of that neuron.

A popular choice for NAF is the sigmoid function defined by

$$y_j = \frac{1}{1+e^{-\lambda s_j}} \qquad , y_j \in \{0,1\}$$

The above expression exhibits logsigmoidal behaviour which is used for the neurons which produce unipolar output i.e. $y_j \in \{0, 1\}$. Bipolar output can be realized using tansigmoidal activation function. The use of sigmoidal functions is biologically motivated, since it attempts to account for the refractory phase of real neurons [1].

Approximate derivative of NAF can be obtained by central difference approximation

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IMPLEMENTATION OF A DETERMINISTIC TRAFFIC REGULATOR

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Abstract

The implementation of the min-plus traffic regulator is aimed to focus on the development of models for VLSI architectures for network elements like traffic shaper, play-out buffers, service curves or schedulers for fixed and variable packet size. The VLSI implementation using HDL facilitates a hardware implementation, which will speed up the smoothening of the traffic in real time. The performance of the regulator on the data can be precisely controlled by choice of proper values of the token generation rate and the buffer size. The scaling of the architecture and the scaling of its data handling capacity becomes realizable once the shaper is implemented using HDL. Hence the shaper can also be used to smoothen VBR traffic and real time encoded data of variable precision. This regulator uses the min-plus algebra in determining its structure.

Key words: *HDLs, Network Calculus, greedy shaper, VLSI architecture, CBR, VBR.*

1 Introduction to ATM networks

ATM (Asynchronous Transfer Mode) has been designated as the target transfer mode approach to provide the desired integration of the various traffic types to be supported by B-ISDN (Broadband ISDN). The packets or cells are assigned on demand at the User Network Interface (UNI). At the User Network Interface, the Leaky Bucket Algorithm, which is both a measuring, and an action algorithm is used for traffic shaping to monitor the traffic. We propose to implement the above using the theory of network calculus to yield deterministic determination of parameters D or ρ and M or σ.

2 Theory of Network Calculus

Network Calculus provides deeper insights into flow problems encountered in networking. We consider a system whose impulse response is h (t). If the input signal is x (t), then the output y (t) of this system is given by the conventional convolution integral

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IMPLEMENTATION OF BLIND ADAPTIVE FILTERING

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Abstract

Noise in any form is Undesirable. The unwanted noise causes irritation. The primary problem faced during noise reduction pertaining to speech, is that no parameters are known about the characteristics of noise. Hence an adaptive approach is an apt solution to this problem [1]. Further a blind technique is well suited in this case wherein no prior assumptions are made regarding the properties of speech and noise [2] ,[3]. The differentiation between speech and noise is made. This characteristic is used to derive a cost functional for speech enhancement. Adaptation is by changing two sets of weights. The simulation and synthesis of the above technique/algorithm is implemented using Matlab, Verilogger pro and Leonardo spectrum. The existing technique used to enhance the speech quality is subject to both degradations due to road, engine and wind noise. All these tasks must be achieved with a single VLSI chip in order for the system to be both cost-effective, power efficient and widely accepted [4]. Hence the goal of this paper is to prove that this technique can better the existing one, using VLSI technology the same can be implemented and realized. It finds its application in Mobile phones (hands-free kits), Hearing aid problems.

1. Introduction

The primary requirement is a strategy by which we will be able to differentiate between noise and sound. This may be achieved by analyzing the properties of human speech. This idea has been put forth earlier [2]. To make the model much more effective, we have tried to implement it using VLSI technology.

2. Strategy For Noise Identification

We express the incoming signal as y[n] which is a combination of speech s[n] and noise u[n].

$$y[n] = s[n] + u[n] \quad (1)$$

No prior knowledge about the parameters of s[n] and u[n] are known. we described some of the important features of the human speech signal s[n]. However, the characteristic that plays prominence is its non-stationary nature while considering a time frame of over 250ms. In this same time frame noise is predominantly stationary in nature. For noise, the autocorrelation structure and the power spectrum density remains constant over long time intervals. This basic property is used to differentiate between noise and speech. [5].

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VLSI Design Simulation for Routing in Communication Network using Parallel Architecture

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ABSTRACT

This paper proposes a new VLSI design by modifying the existing routing algorithm [2] in communication network, which can handle path reliability with enhancement in processing speed. The neural network based algorithm is implemented in VLSI design using parallel architecture. The purpose of this architecture is to enhance the processing speed which makes the router as a efficient device. The speed is enhanced by the parallel architecture and modification done in initialization of weights for iteration in the algorithm. The unreliability factor for each node and the whole path is considered to find optimized path and sub optimal paths. Simulation results are included to prove the effectiveness of the design.

1. INTRODUCTION

Communication network has been undergoing major changes in network architecture and services. Network must be designed for flexibility adaptability with respect to access topology, routing and demand patterns. Under the failure condition, the information of the shortest path table must be updated by reconsidering the new state of network in the routing algorithm. Many traditional algorithms have several drawbacks. These drawbacks are overcome in the algorithm [2], which computes by considering node reliability. But the proposed work discusses with path reliability. Neural network[3] approach is used in this algorithm.

2. PROBLEM FORMULATION

A communication network is usually modeled by a stochastic graph G~(V,E), where V and E are sets of nodes(vertices) and links (edges) of G. Before stating the problem, we first define certain parameters. They are as follows: s- source node, t- destination node, n- number of nodes in the network, h- maximum number of links of optimal paths from s to t. c_{ij} - capacity of the link from node i to j which is represented by n x n matrix. q_i – Failure probability of node i and represented by n x1 matrix.

Once th[1]e optimal path is formed, the path reliability can be calculated by using following relation.

$$q_p = \Pi_{i=1}^{m} q_i \qquad (1)$$

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COMPARATIVE ANALYSIS OF FPGA PERFORMANCE

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Abstract: A comparative study of some FPGAs and PLDs manufactured by various companies have been attempted in this work. We designed a third order Chebyshev filter and synthesized the digital design in various technologies available in FPGA. After analyzing the delay and area consumption statistics, an area-delay normalized index is developed and comparative study of these technologies is made.

Index Terms: Field Programmable Gate Arrays, Programmable Logic Devices, Area, Delay, area-delay index, Chebychev filter, adder, multiplier.

1. Introduction:

For prototyping and for applications where specialized chip requirement is low FPGAs are very useful. It has been found out that various modeling styles of FPGA building blocks exist [1,2,3]. However, comparative information of various FPGAs in terms of area, speed, cost and power consumption is generally not available. In this paper, we have analyzed various FPGAs available, in terms of area and speed.

Third order digital filter has been chosen for the analysis. The basic building blocks of any digital filter are multiplier, adder and registers. Various adders and multipliers are studied [4,5,6]. Using a fully optimized Wallace tree implementation for multiplier, the chosen filter is synthesized into various FPGA technologies (devices) available in Leonardo Spectrum, a synthesis tool. Area occupied by the design and area-delay product are two criteria chosen for the analysis of the results obtained from simulation.

Section 2: 3RD Order Chebyshev filter

We have chosen a Chebyshev Filter that has minimum pass band ripple of 1.2 dB and attenuation of at least 25 dB at ù=2.5. The transfer function is given by

$$G(s)=\frac{f}{(s+0.4606)(s+0.2303-j0.9534)(s+0.2303+j0.9534)}$$

FULL CUSTOM VLSI IMPLEMENTATION OF GOLAY AND EXTENDED GOLAY ENCODER AND DECODER

Annajirao Garimella [1]

Abstract

Golay code is a cyclic linear block code used for error detection and correction during the information transmittal over a channel. In this paper, full custom VLSI implementation of binary Golay and Extended Golay Encoder and Decoder is presented. MAGIC is used for layout and SPICE3 is used for simulation. Special pitch matching techniques have been used for the layout. Both the designs are compared for the area, transistor count and efficiency.

1. Introduction

In this paper Full Custom VLSI implementation of Golay and extended Golay codec is presented. Section 2 gives the background and discussion on Golay and Extended Golay Code. Full custom VLSI implementation details were presented in Section 3 and Section 4 summarizes the results along with applications of Golay code and the future strategies.

2. Golay and Extended Golay Code

Golay codes are linear block based error correcting codes. An (*n, k*) linear block code takes blocks of *k* information bits and generates blocks (codewords) of n bits. The *n – k* extra bits are called parity bits.

$$c = \underbrace{p_0 p_1 \cdots p_{n-k-1}}_{parity\,bits}\ \underbrace{a_0 a_1 \cdots a_{k-1}}_{message\,bits}$$

Here the uncoded data word vector matrix A of size $1\times k$ can be given by

$$A = \lfloor a_0 \quad a_1 \quad . \quad . \quad . \quad a_{k-1} \rfloor_{1\times k}$$

An (*n, k*) linear block code is characterized by the following.

a) Code rate: $R_e = \frac{k}{n}, 0 \le R_e \le 1$

b) Minimum Hamming Distance: $d_{\min} = \min d_H(c_i, c_j)$

c) Correction capability: $t = \left\lfloor \frac{d_{\min} - 1}{2} \right\rfloor$ errors

d) Detection capability: $v = d_{\min} - 1$ errors

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Application of Non-Equilibrium Green's Function Formalism for Nanometric MOS Device Modeling and Simulation

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Abstract

Quantum Mechanical effects (QMEs), which manifest when the device dimensions are comparable to de-Broglie wavelength of electron, are becoming common physical phenomena in the current nano-meter technology era. While most devices take advantage of QM effects to achieve fast switching speeds, miniature size and extremely low power consumption, the mainstream MOS (Metal-Oxide-Semiconductor) devices (with the exception of EEPROMs) are generally suffering in performance due to these effects. Solutions to minimise the adverse effects caused by QM while keeping the down scaling trend (technology feasibility aside) are sought in the research community and industry wide. For MOSFET, QM effects strongly influence the device parameters and the output global characteristics, which manifest in the form Drain Induced Barrier Lowering (DIBL) and other Short Channel Effects (SCEs). These QMEs also affect the global output characteristics of the device to a large extent. MOS transistors with channel lengths as low as 15 nm and below are now been actively studied both theoretically and experimentally [1]. At the same time recent demonstrations of molecular switching make moloecular electronic devices seem a little closer to reality. It is clear that quantitative simulation tools for this new generation of devices will require atomic-level quantum mechanical models. The non-equilibrium Green Function (NEGF) formalism provides to a large extent a sound conceptual basis for the development of this new class of simulators. Although transport issues in MOS transistors or molecular electronics are completely different, the NEGF formalism should provide a suitable conceptual framework for their analysis as well. In this paper, a self-consistent solution of quasi two-dimensional Poisson's equation and Schrodinger Wave Equation (SWE) is done to evaluate the output characteristics of a nano-scale MOSFET (gate length = 10 nm)

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EFFICIENT HARDWARE IMPLEMENTATION OF DCT ALGORITHMS FOR IMAGE PROCESSING

Sigu Joseph[1]

ABSTRACT

In order to conserve communication bandwidth, compression technologies incorporating signal transforms like DCT are employed. In this paper we are going to compare between various DCT algorithms (both 1-D & 2-D) & suggests an efficient restructured algorithm (1-D) which is highly suitable for hardware implementation. Simulation /Verification is done in Altera MAXPLUS+II, the target chip is ACEX 1K EPIK100QC208-1. It is worthwhile to note that all registers are 100% utilized. The restructured butterfly position gives us reduced time of operation.

1) Comparison of 2-DCT Algorithms

1.1 Row-Column Decomposition method [4]
1.2 Vector Radix method [4]
1.3 Polynomial based algorithm for 2 D-DCT
1.4 Fast DCT algorithm (FCT) [1]

Table –1

Comparisons in terms of number of additions, multiplications &Regularity

Algorithm	✻	+	**Regularity**
Fast 2 D-DCT	96	466	Good
Row Column	192	464	Good
Vector – radix	144	464	Average
Polynomial	96	484	Poor

Looking into the table it is easy to make an **engineering judgment,** so that fast 2D- DCT to be the algorithm for hardware implementation.

2) Comparison of 1D-DCT Algorithms

2.1. Trial of DCT through FFT method
2.2 DCT through FFT Method [4]
2.3 Fast Cosine Transform Method:[2]

Table –II

Overall comparison between the 1-d DCT algorithms:

Algorithm	✻	+	Regularity	Stages
FCT	12	29	Good	5
DCT thru FFT	17	24	Average	4

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CMOS CAMERA WITH ELECTRONIC SHUTTER

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Abstract: A 256x256 monochrome active pixel image sensor with electronic shutter is designed in 0.35µ, 1 poly and 4 metal, digital CMOS technology. The pixel consists of 4 NMOS transistors and a photodiode with reduced electrical coupling. Each pixel is 10µm by 10µm and has a fillfactor of 35%. The signal from pixel is readout as voltage. Correlated Double Sampling (CDS) is used to reduce fixed pattern noise (FPN). Camera is designed for optical dynamic range of 60dB.

Introduction: The demand for low cost, low power, compact image acquisition system for multimedia, mobile applications have blown through the roof. The industry and market looks forward to a single die solution i.e. image acquisition and signal processing on same chip. Presently used Charge Coupled Device (CCD) technology does not satisfy the above needs and also suffers from other disadvantages [1][2]. The paper discusses CMOS camera that satisfies the above needs. Although it suffers from more noise but off-chip and on-chip DSP techniques can be utilized to reduce noise levels [3].

Camera Architecture: Figure 1 shows the architecture of CMOS camera.

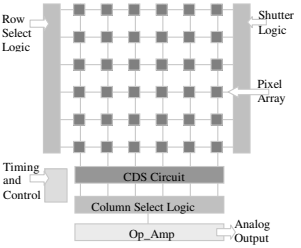

Fig 1 CMOS Camera Architecture

The pixel array forms core of the image sensor. A row of pixel is selected at a time using row decoder. The pixels are readout through the vertical wordlines which are connected to CDS circuitry for respective columns. Output from the row of CDS circuitry are multiplexed out via a analog multiplexer to input of an

A Fast 16-bit TSPC Adder in SOI CMOS

Lakshmikantha Holla V, Prasant Vallur, Poras T Balsara,
Aravind K Navada, Shashank Shastry [1]

Abstract

Low latency and high performance can be achieved in a pipelined Carry Lookahead Adder (CLA) by utilizing the unique properties of Partially depleted SOI (PD-SOI). Utilizing deep stacking possible in PD-SOI and True Single Phase Clocking (TSPC) logic design style, we demonstrate a 5 stage (3-clock cycle latency) 16 bit CLA operating at 4.03GHz. This circuit works 2 times faster than an equivalent bulk CMOS implementation and consumes lesser power.

1. Introduction

Circuits implemented in SOI CMOS technologies have proved to be very attractive for high-speed applications [Shahidi, Oct 99]. Arithmetic circuits with low latency and high speed are necessary in the quest for higher speeds in microprocessors and DSPs. TSPC logic style is a preferred logic design style used to obtain high speed in addition to avoiding clock skew, overlap and feed through problems that are characteristics of dynamic circuits [Yuan and Svensson, 1989]. The speed advantage for this CLA comes from two primary factors. Firstly, deep stacking of transistors in SOI circuits enable block level Propagate and Generate equations for higher order CLA to be implemented easily, by reducing the number of stages in it. Also reduced in the process are the number of latches and clock tree buffers. Secondly, TSPC logic style ensures very low propagation delays for these highly stacked structures. The end result is that a pipelined 16 bit CLA with a latency of less than 3 clock cycles (5 stages) operating at clock speed of 4.03GHz is obtained.

2. CLA Design

A fully pipelined 16-bit CLA can be constructed in 9 stages with a blocking factor of 2. Blocking Factor is the number of bits combined in a block per stage to form a group generate (G) and a group propagate (P). This architecture has a latency of 9 clock edges if logic evaluation is done on every clock edge. A higher blocking factor results in lesser number of stages. We demonstrate this fact by examining a section of the 16-bit CLA, namely the generation of carry signal c_8. With a blocking factor of 2 (Figure.1), the equations are:

$$X1:\ p_i = a_i \oplus b_i;\ g_i = a_i * b_i;$$

$$X2:\ G_{k.i} = G_{k.j+1} + P_{k.j+1} * G_{j.i};$$

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Carry circuitry for LUT-based FPGA (optimized for implementing finite field multipliers)

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Abstract

This paper presents a carry chain which is optimal for implementation of finite field multipliers. This kind of architecture will be very useful for designs which have very large number of mathematical operations in it. Encryption is one such field of interest where large amount of finite field computation is required. Higher performance can be achieved by prototyping such designs by using the below discussed architecture. The aim of this architecture is to accommodate as much logic as possible in one LUT without increasing the size of the LUT proportionately. The discussed carry chain designed for 3-input LUTs.

VLSI IMPLEMENTATION OF IMAGE RESIZING ALGORITHMS: ISSUES AND PROPOSED SOLUTIONS

Indu. S. [1], Avinash K. R. [2]

Abstract

Resizing of digital images is desirable in the areas of digital communications where images are required to be transmitted over communication channels of varying bandwidths. The image resizing is also desirable where we need to display the images at different resolutions depending on the resolution of the display devices. The present work explores the VLSI implementations of image resizers for different imaging systems for real time processing. The image resizing typically involves the re-sampling of the input image data. The hardware implementations for these image-resizing algorithms invite special attention. This is so because even the fractional re-sampling of the images may lead us to prohibitively large hardware implementations. The image resizing algorithms have been proposed to resize the images in spatial domain [4], as well as in the frequency domain [1-3]. The image resizer's in spatial domain are usually implemented as polyphase interpolators and decimators. These structures inherit the problems of considerable memory overhead and the insertion of a number of frame latencies. This work presents and discusses these problems and introduces a novel DCT based system level architecture of an image resizer to overcome these problems.

Keywords: Image Resizing, DCT, FPGA

1. Introduction

Image Resizing is used to change the size of an image. This is required to display the images at different spatial resolutions because the same source image may be required to be displayed on different display devices. Also the progress in the area of video and image compression techniques has reduced the bandwidth requirements for video communications thus enabling video conferencing, video broadcast and video wireless applications. With this continuous growth in the video communication industry the different size and orientation of the images is a noteworthy problem to address. In many internet applications such as e-cards, it is first preferred to see the down sampled image first and depending on one's interest the original image or upsized image is downloaded.

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DESIGN FLOW AND METHODOLOGY FOR 50M GATE ASIC

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Abstract

This paper presents a methodology for full chip RTL timing closure for very large ASIC's. The methodology is based on the concept of a "Silicon Virtual Prototype". The methodology is based on the scalable technique of clustering and cluster placement and leverages the tight integration between the algorithms by means of a common, unified data model.

1. Introduction

The complexity of today's largest IC designs is over ten million gates. Looking ahead it is prudent to prepare a methodology for the 50M gate ASIC. Three forces are at work which make designing chips at the edge of the capability of the fabrication technology increasingly difficult. First, the size of today's 10M gate designs taxes even the largest and fastest computers. Second, the deep sub micron (DSM) effects are breaking existing design flows. The third force is the shrinking market window. The capacity and complexity problems impact the productivity causing a product to miss its market window.

This leads to a requirement for a **fast, high capacity and scalable** technology that provides early estimates of post-layout performance and identifies many issues that would typically have been found only after detailed place & route in a conventional flow. This saves numerous time-consuming iterations and enhances the productivity to enable fast time-to-market. An additional advantage of such a technology is that engineers can explore design architectures and implementation alternatives and have a high level of confidence that performance goals can be achieved.

The approach being discussed in this paper is that of a silicon virtual prototype (SVP). A *silicon virtual prototype* is a fast physical implementation of the design. This implementation has been coarsely tuned to reduce some of the most time consuming analyses and optimizations. However, the silicon virtual prototype still has sufficient accuracy to identify long-wire type timing implementation issues that are prevalent in large designs. Virtual prototyping leverages its high capacity to have a global view of the chip design to identify problems and also automate the creation of a floor plan. While most of the steps can be done automatically, the opportunity for manual intervention exists in most intermediate stages. Thus, the process of quickly building a virtual physical prototype of the final design from RTL or netlist in order to estimate chip area, performance and power early in the design cycle and determine changes needed to the RTL or constraints, if any, in order to successfully achieve timing closure in implementation, is called silicon virtual prototyping.

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Seamless Physical Design Flow – Challenges and Solutions

Abhishek Pandey[1], Pradeep Cavale[2], A. Krupakaran[3]

Abstract

Design flow automation continues to predominate the world of VLSI design. EDA vendors continue their focus on developing end-to-end solutions. While there are many popular tools and sub-flows, there is no single framework which can claim to represent the design flow from RTL to GDSII. There are few leading tools in different segments of the flow but flow definition and integration for a design is usually a tedious task requiring specialists to mix and match the tools to get the most optimum design flow for a design. We are trying to address this space in this paper. We hereby present a revolutionary system called *QuickFlow* (QF). QF provides a seamless flow to take a design from RTL to GDSII, by allowing creation of flows based on a mix of preferred tools. Utilization of resources (servers, licenses) will be efficient and it captures reuse within the system. QF is easily customizable to new and emerging technologies like 0.13/0.09 um and above and to specific foundries. An expert system based learning is available to help users choose tools/flows for their specific purpose. Project Management capability is included within the system. All these features come with a web based control to the system for initiating and monitoring tasks. We also present the benefits we have seen in using such a system with a sample application to a 0.13 um flow. The scope for future work includes improving the learning capabilities of such a system. The end goal is to have a system which provides expert guidance for the user while building his system and provide all the necessary feedback with quantifiable metrics required for him to improve his flows and eventually cut down his design cycle time. While this system has been targeted for now on the Physical Design aspect of VLSI, the concepts are generic and can be applied to front-end or other design flow segments as well

1 Introduction

It is a well known fact that design teams constantly upgrade to new tools and flows. The driving factors behind this are increasing design complexities, new technologies or partnerships with new EDA companies. In this scenario, we have several tools/sub-flows that need to get stitched together to provide a seamless flow. Every time there is a shift to a new flow, there is a need for the Flow definition and Validation by an expert and new users need to be trained by the expert. Flow creation and execution becomes more difficult when we try to use tools from different vendors. It is a challenge to make new tools work

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Partitioning of Circuits for Mapping onto Dynamically Reconfigurable FPGAs

K. Suresh and Santanu Chattopadhyay[1]

Abstract

Dynamically Reconfigurable FPGAs (DRFPGAs) have become an active area of research for reconfigurable computing, due to their potential to dramatically improve logic density by time sharing logic. Partitioning in DRFPGAs is different from the traditional partitioning problems due to the precedence constraint among the nodes. In this paper, we use simulated annealing technique for partitioning combinational circuits onto DRFPGAs, which can handle the precedence and capacity constraints while minimizing the cost of interconnections between different stages. The algorithm is tested on the MCNC Partitioning93 benchmark circuits.

Introduction

Frequently, the areas of a program that can be accelerated through the use of reconfigurable hardware are too numerous or complex to be loaded simultaneously onto the available hardware. For these cases, it is beneficial to be able to swap different configurations in and out of the reconfigurable hardware, as they are needed during program execution. This concept is known as run-time reconfiguration.

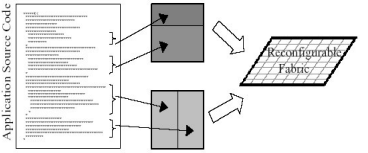

Figure 1: Run Time Reconfiguration

Dynamically Reconfigurable Field Programmable Gate Arrays (DRFPGAs) have become an important research topic for reconfigurable computing due to its

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A Unique Method For Dynamic Voltage Drop Analysis and Decoupling Capacitance Estimation

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Abstract

*Simultaneous switching in core circuitry with in short period of time causes large current spikes in the Power/Ground networks that can cause considerable dynamic voltage drop over the power grid. Dynamic voltage drop (power supply noise) includes time varying i(t)*R voltage drop due to power grid resistance and Ldi/dt (Delta-I noise) due to package inductance.*

Power supply noise degrades the performance of the chip. In this paper, we propose a unique method for dynamic voltage drop analysis based on RLC models for off-chip package and on-chip power grid. We also propose an equivalent switching circuit model representing the entire chip along with intrinsic decoupling capacitors (DECAP). DECAP must be optimized to supply the peak charge while keeping dynamic voltage drop less than allowed threshold. We also propose (DECAP) estimation and placement methodology for inserting DECAP

Index terms—*Ultra Deep Sub-Micron (UDSM), Power and Ground (PG) networks. Decoupling Capacitance-DECAP.*

1. Introduction

Power Bus Integrity is one of the most important issues impacting today's high density and high performance UDSM designs. Power supply noise is a critical problem in the power integrity domain. Power supply noise happens due to simultaneous switching in the chip which causes large current spikes in the power and ground network. The dynamic voltage drop includes i(t)*R due to power grid resistance and Ldi/dt over the PG networks due to on-chip and off-chip inductance. On-chip inductance is due to power grid and off-chip inductance due to bond wire, package, board and power supply. In this paper we describes the off-chip package level. In current designs on-chip inductance can be ignored, as it is negligible compared to package.

Power supply noise degrades the drive capability of the transistors due to reduced effective voltage seen by the transistors and hence increases the delay that can cause chip functional failure. Power supply noise degrades the performance and reliability of the chip [1][8].

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USEFUL SKEW MANAGEMENT INSIDE STANDARD CELL LIBRARY

AMOL BIDVE:[1] PANKAJ ROHILLA:[2]

Abstract

Clock scheduling (useful clock skew) is seen as one of the solutions for many problems like speed limitation, Peak currents near clock edge. Still its implementation is a tedious and complex process. In this paper we propose a method to implement useful skew in a very simple way bypassing all implementation flow problems. As useful skew is applicable only when there is time space available in sequentially adjacent paths. Delaying first capture edge gives us more time for first data path. We propose to introduce this required skew in first capture flip-flop itself. Having such flipflops with negative setup time available in library enable synthesis to instantiate such flipflops where there is scope and need to introduce skew. This also helps to reduce drives of cells in first datapath and probably reduce the power consumption. In some cases it is seen that this drive reduction of datapath cells resulted in over all area reduction inspite of increased flip-flop area. Although speed improvement may not be always possible because of timing critical sequentially adjacent paths there can be significant reduction in high drive cell usage, total number of cells and & sometimes reduction in total area.

1. Introduction

Most of the methods proposed for useful skew implementation are proposals to implement the same in physical implementation flow, Which not only is seen by may of the designers as design overload and also an additional risk in implementation unless the designer is pretty experienced (for which many times the idea is discarded and other ways like choice of some new process or fast logic consuming more resources are opted). Result we see is, although most of the advanced tools support his optimization technique its usage by average users is negligibly small. We propose a method, which enable all users to use this concept with no hesitation. This proposal actually hides the useful skew being used from semi custom designer. And still it provides all benefits of useful skew. In this paper we elaborate on the concept and our experience for usage of such special cells in present day design tools. Also we

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LOW POWER AREA-EFFICIENT DIGITAL COUNTERS

Chandra Mohan Umapathy[1]

Abstract

The thrust of today's digital design is to achieve high speed, low power and more dense circuits. This paper proposes a novel architecture for low power digital counters, occupying less area & achieving speeds equivalent to that of one-hot coded counters. Comparison is made between different implementations of the counter. The simulation results show an improvement in performance in terms of area & power while keeping the timing intact, when compared to any of the designs referred in this paper.

1 Introduction

Traditionally the constraints for a design were Speed & Area. In the recent mobile & portable electronic age, the need for low power design is posing a great deal of challenge to the Chip designers. The increase in the use of the battery operated devices for personal communication has forced the designers to give more importance to the low power designs. So in short, the key concepts that are driving the low power designs are Portability & Mobility. Power consumed by certain logic is determined by the number of times the output toggles for a given interval of time. Generally, the power is specified in terms of the number of transitions that occur inside a logic within a certain amount of time. Usually, it is seen in most of the cases that power is directly proportional to the area (apart from some exceptional cases).

The paper is organized as follows: the first section gives a brief introduction of the different aspects & the motivation for the Low Power & Area Efficient designs. The second section reviews the basic need of counters & different methods of implementing counters. The third section introduces a new concept of designing counters, which occupy less area & consume less power. The fourth section deals with the comparison of the proposed architecture with the traditional method.

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Design Challenges: Virtual Concatenation, Next Generation SONET/SDH

Nikhil Bhatia*

Abstract

To support the massive Internet expansion of recent years, carriers significantly increased the capacity of backbone and core networks. Metropolitan area networks (MANs), however, have not kept pace with this growth, creating a bottleneck in the overall network infrastructure. Carriers built the metro using mature Sonet technologies, which, while optimal for voice or other jitter- and delay-sensitive applications, lack fast circuit-provisioning capabilities, scalability and bandwidth efficiency. This makes the MAN inefficient for the cost-effective transport of data. Carriers looking to reduce capital expenditures, while meeting the demands of data traffic growth and new service offerings need to extract maximum value from their existing networks. Emerging mapper/framer technologies, such as virtual concatenation, enable carriers to upgrade their existing Sonet networks with minimal investment. These technologies can help increase carriers' profitability by enabling new services through greater scalability, faster provisioning and much higher efficiency when transporting Ethernet over Sonet and packet over Sonet data.

Designers at the chip, equipment, and carrier level have touted the wonders that virtual concatenation delivers, what often gets lost are the real challenges that chip and equipment developers will face when implementing virtual concatenation in a real-world design which we intend to discuss in this paper.

Introduction

Why VC is so hot!

Much has already been said and written about the benefits of virtual concatenation over current payload mapping capabilities of Sonet and SDH. **Table 1** summarizes the individual payload capacities of different commonly used Sonet or SDH paths. The table includes both high- and low-order paths with and without standard contiguous concatenation (denoted by the "c"). While allowing a range of bandwidths to be provisioned, these current mappings do not have the granularity required to make efficient use of the existing network infrastructure. One other important point to note is that contiguous concatenation of VT1.5/VC-11s or VT2/VC-12s is not supported.

Table 1: Current Sonet and SDH Payload Capacities

Container (Sonet/SDH)	Type	Payload Capacity (Mbit/s)
VT1.5/VC 11	Low Order	1.600
VT2/VC 12	Low Order	2.176
STS-1/VC 3	High Order	48.384
STS-3c/VC 4	High Order	149.76

Making Use of Unused Overhead : In addition to allowing more flexible mapping, virtual concatenation also releases two of the restrictions upon which

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The Energy Impact of Memory Port Allocation Decisions

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VLSI Design and Test Workshop (VDAT)
Bangalore, 28-30 August, 2003

POWER MANAGEMENT IN EMBEDDED SYSTEMS BY AN EFFICIENT ONLINE IDLE TIME PREDICTION SCHEME

*** Rajeswari .P, **[1]Lakshmi Prabha. V, *** Elwin Chandra Monie**

Abstract

Dynamic Power Management (DPM) is an important technique to reduce power consumption in embedded and portable systems. Power hungry devices such as disk drives, network interfaces and other peripheral devices are often designed with multiple power saving states, and control knobs are provided for changing their power states under the operating system control. DPM strategies are "Online" strategies since they must make decisions about the timing of transitioning to lower power consumption states during idle periods without knowing when the next request for service will arrive. In this paper we present a new approach to designing adaptive online DPM strategies. This approach dynamically learns the probability distribution of idle period lengths from recent request patterns. A probability based scheme then uses this information to optimize power saving actions. Our study includes measuring power usage as well as additional latency introduced from the delay in powering back up when a new request for service arrives and comparing our strategy with various previously proposed strategies.

Introduction:

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Novel Source-Independent Characterization Methodology for Embedded Software Energy Estimation

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AN AVAILABILITY MODEL FOR COSYNTHESIS OF REAL TIME SYSTEMS

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Abstract: The co-synthesis of hardware-software systems for distributed and/or embedded applications has been studied extensively in the recent past in combination with various qualitative objectives. However, the problems related to design exploration with the specific objective of achieving the desired levels of availability in a gracefully degrading system need to be addressed systematically. In this paper we propose an availability model which captures, within a flexible rule-based framework, the user and context determined availability requirements of a real-time task graph. The model is applied for the co-synthesis of heterogeneous, multiprocessor architectures with optimized performance, availability and cost attributes, The technique considers stochastic task graphs with soft deadlines and employs a genetic algorithm (GA) to optimize the resource selections, task allocations and task schedules. Results on a set of task graphs show that it is possible to obtain a set of near-optimal solutions offering a range of performance and availability benefits at different costs.

Keywords: Reliability and Availability, Graceful degradation, Hardware software co-synthesis, Task allocation and Scheduling, Stochastic Task Graphs, Genetic algorithm based optimization, Real-time systems

1. Introduction

Reliability is an important and highly customer oriented measure of quality for distributed and/or embedded real-time systems[1]. Today's complex applications such as airflight control and robotics rely heavily on the hardware software co-design of heterogeneous multiprocessor systems which typically integrate a range of processing units such as programmable processors, ASICs and FPGAs. In such systems, failure of a part of the system does not render it totally useless. The system can still be of value to the users, though at a degraded level of performance [2]. Therefore Reliability and Availability (R & A) must be considered in the context of systems which can deliver multiple states of service. A crucial design decision is to determine the most cost effective way of allocating the available resources to support the various sub-tasks of an application, so that the system continues to provide core services and the most important user needs are sustained. In this paper, we tackle the problem of capturing the user-determined availability requirements for a system with degradable performance and using them to construct heterogeneous architectures with high levels of performance and availability. The rest of the

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RECONFIGURATION IN SOC WITH PROGRAMMBALE INTEROCNNECT

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Abstract

The continually increasing integration density of integrated circuit, with astronomical increase in fabrication cost and enormous time to market, portrays important paradigm shift in next generation system-on-a-chip [SoC] design. This leads towards more programmable designs that can spin a wide range of applications. Hence, there is a trend away from the fixed SoC to highly flexible SoC with improved time to market. The reconfigurability in SoC can be achieved either by the programmable gate arrays [FPGA] and/or through programmable interconnect. The emergence of static memory based FPGA that are capable of being dynamically reconfigured i.e. partially programmable during runtime has been a driving force for flexible architecture. At the same time, the standardization of the intellectual property [IP] deliverables and their wide availability has started gaining the importance towards expanding the possibility of reconfiguration in SoC. Synthesis of SoC has become less complicated, shortening design time, with the IP reuse, which could be achieved by socketization. The pre-designed and pre-verified IP blocks are obtained from the internal sources or third parties, and combined onto a single chip. This arises a need of rapid integration of communication between different modules embedded in the system. The paper provides an overview of interface strategy, which suggests dynamic plugging of varying IP blocks; with the aid of programmable interconnect, to enable ever-changing system that can be adapted to almost any requirement for SoC; reconfigurable pipeline data paths [RaPiD] and advance micro controller bus architecture [AMBA]. This paper also tries to introduce some of the important issues surrounding them.

Keywords

System on a chip, reconfiguration, programmable interconnect.

Introduction

System on a chip (SoC) have been in existence for only a few years, however in that span of time, the definition of the 'system' designed and manufactured on a chip has significantly changed and expanded as did the technology, skills, tools and methodologies required to produce it. Today, SoCs are often mixed technology designs, including such diverse combination as embedded DRAM, high performance and low power logic, analog and RF blocks. But this progress raises its problem, e.g. it takes enormous amount of time and effort (-> cost) to design and integrate a chip [9,12].

STATIC APPROACH FOR PEAK POWER SUPPLY NOISE ESTIMATION

Ananth G Somayaji[*], Gaurav Thareja[*], Gautam Kapila[*], Vikash Rakhecha[*]

Abstract

As voltage and device feature size continue to scale down, voltage drops along power and ground networks are emerging as a major challenge for high-performance circuits. Excessive voltage drops manifest themselves as glitches on the PG (Power Ground) buses and cause erroneous logic signals, degradation in switching speeds, reduction in Noise Margin and Driving capability of the gates. It is imperative that a designer has an automatic and reliable flow, which will help him analyze the power rails for large power dissipation. In particular, the Dynamic PG Noise due to simultaneous switching (including power droop and ground bounce) and Off-Chip Ldi/dt noise is becoming the dominating component of the total noise. Accurate estimation of the worst-case PG Noise is very difficult due to innumerable possible combinations of the input vectors. Creation of a realistic set of worst-case input stimuli and hence estimation of the worst-case full-chip dynamic PG Noise is therefore both impractical as well as computationally infeasible. The present day multi-million gate designs would need enormous runtime for such an analysis, which would directly impact time-to-market Hence, an input independent approach is much more preferred as a solution to this problem. It would enable the designer to do a worst-case voltage drop analysis as early as the global route stage, thus gaining precious cycle time. It would also avoid unnecessary redesign of PG network later in the design. In this paper we propose a Vectorless approach (Static Approach for Peak Power supply Noise Estimation- SAPPNE) to find the worst-case power supply noise, within the bounds of runtime imposed by the market.

1. Introduction

Currents flowing in the power and ground (P&G) buses of CMOS digital circuits affect both circuit reliability and performance by causing excessive voltage drops. Supply Voltage waveform are needed at every contact point in the buses to study the severity of the voltage drop problems and to redesign the power supply lines accordingly. These waveforms however depend on the specific input patterns that are applied to the circuit. Apart from being

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Memory Architectures for Multiprocessor Embedded Systems

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Micro Electro Mechanical Systems (MEMS) : An Overview

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Deep Sub-Micron CMOS - Reliability Issues

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VDAT 2003 – Tutorial

28 August 2003, Bangalore, India

Output Structure For Visible Imager Charge Coupled Devices

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ABSTRACT

Charge Coupled Devices (CCDs) are being widely used for imaging applications. In case of visible imagers, the photodiodes are integrated along with the CCD shift registers on the same chip. Apart from photodiodes and shift registers, suitable output amplifiers are also required. The output amplifier senses the charge from the shift register and converts it to voltage for further processing by the external circuitry. The main objective of the on-chip amplifier is to provide a link between a very sensitive charge detection node and the signal processing circuitry external to the CCD chip. The amplifier should have high gain, high input impedance, low output impedance, high frequency response, low distortion, low noise and low power consumption.

The charge detection circuit is shown in Fig. 1. The circuit comprises of an output diode (floating diffusion), a reset transistor and two MOS source follower stages, each comprising of an active transistor and a load. At the beginning the potential on the output node capacitance is reset to the reset drain bias (V_{DR}) by applying reset clock (ϕ_R). The signal charge is then transferred to the output diode from the last element of the shift register by the transport clock which causes change in the output diode potential. This change in potential is sensed by the source follower amplifier.

Two stage source follower is used here to have low output impedance and large bandwidth. Depending upon the sizes and types of various transistors, the performance of the

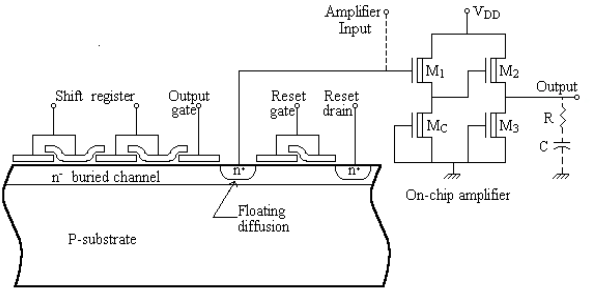

Fig. 1. *Schematic of the CCD output stage.*

MODELING AND SIMULATION OF QUANTUM DOT CELLULAR AUTOMATA (QCA) FOR FUTURE NANOMETRIC DEVICES

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Fabrication of Silicon Membrane at the Free End of Cantilever by Wet Anisotropic Etching

D. K. Maurya, K.Biswas, S.Das and S.Kal[1]

Abstract: Thin silicon membranes are required for realization of various microsensors such as temperature sensor, thermocouples, and pressure sensor. This paper presents the fabrication of silicon membrane at the free end of cantilever by wet anisotropic etching of silicon using 44wt% KOH at 70• C. Time etch stop mechanism has been used to control the silicon membrane thickness. The dimensions of the fabricated cantilever beams are 10mm X 2.5mm X 0.275mm.The membrane dimensions which have been fabricated at the tip of cantilever, are 2mm X 2.5mm X 0.025mm. A 1.3i m thick thermally grown silicon dioxide has been used as masking material during KOH etching.

Keywords: *Silicon membrane; anisotropic etching; Time Etch stop*

1. Introduction

Anisotropic etching of silicon is an important process step in silicon micromachining technology for fabrication of various high precision, miniaturized, complex, high aspect ratio 3-D structures such as membrane, cantilever, v-groove, channels, nozzles [1]. Realization of various micro-electromechanical systems from silicon substrate by bulk and/or surface micromachining technology have been possible because of certain etching characteristics which are unique in single crystal silicon. The most important etching characteristics in silicon is its strong dependence of etch rate on the crystal direction i.e. etch rate will vary for different crystallographic directions. Besides that selectivity of masking material, process compatibility, batch fabrication are some more important issues for silicon micromachining technology. Anisotropic silicon etchants used in micromachining technology are either organic like ethylene-diamene pyrocatocal (EDP), tetra methyl ammonium hydroxide (TMAH), or inorganic etchants like potassium hydroxide (KOH) [2], sodium hydroxide (NaOH), cesium hydroxide (CsOH). The potassium hydroxide solution is the most frequently used anisotropic silicon etchants in MEMS technology. This etchants is well standardized for micromachining process. Although KOH solution has poor etch rate selectivity for Si/SiO_2 over EDP and TMAH etchants. It is most commonly used etchant

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A LASER PRE-AMPLIFIED OPTOELECTRONIC INTEGRATED CIRCUIT (OEIC) RECEIVER BASED ON A SINGLE MESFET FRONT-END

P. Chakrabarti, S. Nayak, D. Mishra and N. Jain[1]

Abstract

The paper introduces a laser pre-amplifier based optical receiver that uses a single MESFET for photodetection and post-amplification. The new receiver can be developed in the hybrid form of optoelectronic integrated circuit using mature InGaAs technology for application in 1.55 μm wavelength region. A theoretical model of the system has been developed to explore the performance of the receiver for the proposed application. Results of our investigation reveal that the proposed receiver exhibits a high sensitivity (exceeding 12dBm at 10 Gbps) as compared to the state-of-the art receivers. The receiver is expected to find application in future generation long-haul optical communication.

1 Introduction

Optoelectronic Integrated Circuit (OEIC) receivers are very attractive for use in long distance optical fiber communication systems. Considerable work has been done in this area over the past decades (Dutta etal (1993); Chandrasekhar et al (1992); Berger et al (1992); Zebda et al (1991); *Nobuhara* et al (1988)). The purpose of this integration is to combine the photodetector and the subsequent pre-amplifier in a single unit. This type of integration improves the speed and reliability of the receivers significantly. Presently used photodetectors include metal-semiconductor-metal (MSM), p-i-n and avalanche photodetectors. The pre-amplifiers are generally based on bipolar junction transistors like heterojunction bipolar transistor (HBT) or field-effect transistor like junction-field-effect-transistor (JFET), metal-semiconductor-field-effect transistor (MESFET), metal-insulator-field-effect-transistor (MISFET) and high electron mobility transistor (HEMT). From the fabrication point of view, it is quite challenging to integrate these two structurally different components monolithically without sacrificing their individual performances. This is because conventional photodetectors have a vertical configuration whereas transistors have a planar one. This bottleneck can be avoided if we could use a detector that has a planar structure like the subsequent amplifier part. Based on this concept, Chakrabarti et al proposed a detector that uses a single MESFET to perform the dual action of photodetection

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CHANNELSORT: A SORTING ALGORITHM BY CONSTRUCTING INSTANCES OF CHANNEL ROUTING PROBLEM

Rajat K. Pal*

Abstract

Sorting is a well-known problem that is frequently used in many aspects of the world of computational applications. Sorting means arranging a set of records (or a list of keys) in some (increasing or decreasing) order. In this paper, we propose a graph based sorting algorithm ChannelSort, where the desired sorted sequence is obtained by constructing an instance of the channel routing problem of VLSI physical design. The algorithm takes time $O(n^2)$ in the worst case, where n is the number of records to be sorted.

Keywords: Sorting, VLSI, Channel routing problem, Channel instance, Complexity.

1. Introduction

There are several algorithms that solve the following *sorting problem* [1]:

Input: A sequence of n numbers $\langle a_1, a_2, \ldots, a_n \rangle$.

Output: A permutation (or reordering) $\langle a_1', a_2', \ldots, a_n' \rangle$ of the input sequence such that $a_1' \leq a_2' \leq \ldots \leq a_n'$.

The input sequence is usually an n-element array, although it may be represented in some other fashion, such as linked list. In practice, the numbers to be sorted are rarely isolated values. Each is usually part of a collection of data called a *record*. Each record contains a *key*, which is the value to be sorted, and the remainder of the record consists of *satellite data*, which are usually carried around with the key. In practice, when a sorting algorithm permutes the keys, it must permute the satellite data as well.

Now there are lots of sorting algorithms in the present day world. Out of which, *insertion sort* takes $\Theta(n^2)$ time in the worst case. *Merge sort* has a better asymptotic running time, $\Theta(n\lg n)$, in the worst case. *Heapsort* sorts n numbers in $O(n\lg n)$ time, whereas the worst case running time of *quicksort* is $\Theta(n^2)$. The average case running time of quicksort is $\Theta(n\lg n)$, though, it generally outperforms heapsort in practice.

Insertion sort, merge sort, heapsort, and quicksort are all comparison sorts: they determine the sorted order of an input array by comparing elements, and it has been proved that heapsort and merge sorts are asymptotically optimal comparison sorts [1].

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A GRAPHICAL USER INTERFACE FOR EMBEDDED SYSTEMS DESIGN

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Abstract

When designing an efficient embedded system, its designer must address several issues, such as the processor, RTOS, compiler, language, power optimization, and code optimization, cost, etc. The designer of embedded system has to consider different parameters for different applications of embedded systems design, which is typical task for him and need more time for design. This tool will helps the designer to arrive his design task easily and effectively with in short time thus it reduces the gap between the designer productivity and transistor density.

Key Words: Embedded systems, RTOS, Micro controllers, Processor, Compiler.

1. INTRODUCTION

An **embedded system** is a combination of hardware and software with some components attached to perform a specific or a narrow range of tasks with limited resources. It is electronic system that is not directly programmed by the user, unlike a personal computer. One of the main ideas of the embedded systems is that the technology used can be very advanced but it is transparent to the user, who can use the system without previous knowledge. Currently, embedded systems can be found in many consumer products that include any kind of electronics. Typical examples go from cars, telephones, elevators, washing machines, toys, to satellites, robots, electronic games, etc. Actually, most of the existing microprocessors or micro controllers are included in embedded systems, more than in general purpose computers. Moreover, the advances in embedded systems technology have a deeper influence in the society than the advances in computer systems for example in the medical electronics, space technology etc.

2. MOTIVATION FOR THE GUI

Embedded System design faces many risks. Projects take too long to get to market. Products that do get to market may fail in the field at great cost to both budget and company reputation. Even exploring whether a design is feasible can cost many months of effort.

Due to their very nature, embedded systems require vertical market expertise, software knowledge, and hardware experience that must all come together in a single solution. Bringing these disciplines together in a combined solution entails design integration challenges that current tool flows simply do not

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PERFORMANCE ANALYSIS OF FPGA

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Abstract: A comparative study of some FPGAs and PLDs manufactured by various companies have been attempted in this work. We designed a third order Chebyshev filter and synthesized the digital design in various technologies available in FPGA. After analyzing the delay and area consumption statistics, an area-delay normalized index is developed and comparative study of these technologies is made.

Index Terms: Field Programmable Gate Arrays, Programmable Logic Devices, Area, Delay, area-delay index, Chebychev filter, adder, multiplier.

1. Introduction:

For prototyping and for applications where specialized chip requirement is low FPGAs are very useful. It has been found out that various modeling styles of FPGA building blocks exist [1,2,3]. However, comparative information of various FPGAs in terms of area, speed, cost and power consumption is generally not available. In this paper, we have analyzed various FPGAs available, in terms of area and speed.

Third order digital filter has been chosen for the analysis. The basic building blocks of any digital filter are multiplier, adder and registers. Various adders and multipliers are studied [4,5,6]. Using a fully optimized Wallace tree implementation for multiplier, the chosen filter is synthesized into various FPGA technologies (devices) available in Leonardo Spectrum, a synthesis tool. Area occupied by the design and area-delay product are two criteria chosen for the analysis of the results obtained from simulation.

2. Third Order Chebyshev filter

We have chosen a Chebyshev Filter that has minimum pass band ripple of 1.2 dB and attenuation of at least 25 dB at ù=2.5.The transfer function is given by

$$G(s)=\frac{f}{(s+0.4606)(s+0.2303-j0.9534)(s+0.2303+j0.9534)}$$

At ù=0 , |G(s)|=1 therefore, the value of f=0.4431. Validity of the design specification was done by the simulation of above transfer function in

POWER OPTIMAL CLOCK DISTRIBUTION IN VLSI CIRCUITS

H.Mangalam[1] and K.Gunavathi[2]

ABSTRACT

Clock networks constitute one of the most important parts of a synchronous VLSI chips as it can significantly influence the speed, area and power dissipation of the system. One major problem associated with clock networks is their power dissipation. Studies have shown that the clock network can dissipate 20-50% of the total power on a chip. Hence it becomes necessary to develop new strategies to significantly reduce the power dissipation of the clock network. In this work, a lower V_{dd} is used for the distribution of the signal over the chip so that the clock network can be made to dissipate less power, while the rest of the circuitry on the chip may use a higher V_{dd} value at the utilization points. Thus this paper presents theory and algorithms for building a low power clock tree. Two low power clock schemes are used: reduced swing and multiple supply voltages.

1.Statement of the problem

In this work, static power dissipation is neglected. The short circuit power dissipation is controlled by enforcing a constraint that the clock edge should never have a transition (rise/fall) time that is larger than a given specification throughout the clock tree. By enforcing this sharp clock edge requirement, the short circuit power is bounded and can be neglected in comparison with the charge/discharge power.

2.Structure of the clock tree

A clock scheme with multiple supply voltages as proposed in [2] is considered and the tradeoffs that are required to determine both a minimum power and minimum area solution are investigated. For the clock tree problem, the use of a driver to drive a long interconnect wire without repeater drivers would result in unacceptable delay and transition times. Hence, a reduced swing clock scheme with drivers, intermediate drivers and receivers is used. The output of the reduced swing driver swings from V_{tn} to
V_{dd}- $|V_{tp}|$. The buffers used ensure a zero steady state short circuit current. The reduced swing receiver is a modified version of a fully complementary self biased CMOS differential amplifier.

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Design and Implementation of Passive RF Tag IC

Sutirtha Deb[1] and Navakanta Bhat[2]

Abstract

A very low power passive RF Tag is designed which contains two sets of data and transmits them selectively according to the requirement of the interrogator. A 2MHz on chip clock generator circuit is developed which provides constant frequency over the operating period even though the stored energy and hence the supply voltage reduces with time. Different blocks get Vdd only when they are operating, in order to save the sleep mode power dissipation, which is very important in the passive tag. Full custom physical design is performed using AMI's 1.5µm technology and the prototype is fabricated through MOSIS.

1. Introduction:

The objective of any RFID system (**Fig.1**) is to carry data in suitable transponders, generally known as Tags, and to retrieve data, by machine-readable means by Reader or Interrogator, at a suitable time and place to satisfy particular application needs. Data within a tag may provide identification for an item in manufacture, goods in transit, a location, the identity of a vehicle, an animal or an individual. By including additional data the prospect is provided for supporting applications through item specific information or instructions immediately available on reading the tag [1], [3].

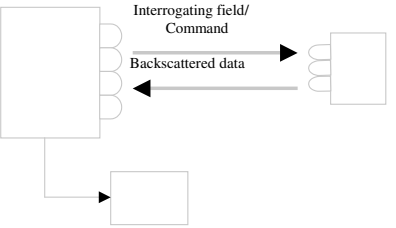

Fig. 1: *Complete RFID system.*

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ARCHITECTURES FOR NOISE REJECTION IN LEVEL SHIFTING LVCMOS INPUT BUFFERS

Author: Vikas Narang[1], Karthik Rajagopal[2]

Abstract

With voltage scaling and increasing circuit design complexity, noise immunity is becoming more and more important. This paper talks about different receiver (input buffer) topologies that provide noise immunity while meeting specs and trading off delay. The paper concludes with a topology that has optimal delay and noise immunity. The topologies have been simulated in TI's 90nm CMOS process.

1. Introduction

As the complexity in circuit design is increasing, the role of a receiver is not restricted to isolating its input and output stages, or to level-shifting a chip level signal to core level signal but also to ensure that a chip level noise should not propagate to the core logic. We need to provide margin for the power supply noise due to Simultaneously Switching Noise (SSN) and cross-talk.

There are a number of ways in which this noise immunity can be improved. We have explored receiver topologies using the methods of DC hysteresis and dynamic hysteresis. We will go into the details of each topology below.

2. Dynamic Hysteresis

A lot of new ideas are emerging for providing the noise immunity in receivers. One of these is Dynamic Hysteresis. Here, the noise immunity is provided during the transition period through a positive feedback without causing any increase in delay.

2.1 Topology-1

Figure 1 shows a receiver topology that uses the concept of Dynamic Hysteresis (Popov and Mollov, 1998). Here, Inverter IHV2 is a low delay Inverter whereas Inverter IHV3 has high delay. Consider the case when INPUT is logic '0' level. Here NMOS1 & PMOS2 will be 'off' while NMOS2 & PMOS1 will be 'on'. Now, when the input starts rising, NMOS1 becomes 'on' as soon as the low delay inverter output (IP3) reaches Vt of the NMOS. Also, the high delay inverter (IHV3) keeps NMOS2 'on' till the transition is over, hence providing a positive feedback that helps node IP2 to reach logic '0' level thus providing the noise immunity during transition period.

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Techniques for Improving the Neural Optimization Method

Atanendu Sekhar Mandal[1] and Basabi Bhaumik[2]

Abstract: For given N points in space Steiner Minimal Trees (SMT) are known to give the optimally connected network. Out of the various techniques available in literature to get the SMT, the neural self organization based optimization technique of Jayadeva and Bhaumik (1994) is a novel one. In this work we have added various features to this neural self organization technique to improve its efficiency.

Keywords: *Steiner Minimal Tree (SMT), convex hull, site points, curve points, partitions*

1. Introduction

Interconnections in VLSI design, and communication networks have assumed a great significance in today's world. The issue is, given a set of points in the Euclidean plane, it is to be connected by the shortest network. The minimal network interconnecting a set of points $A = \{a_1, a_2, ..., a_N\}$ in the Euclidean plane may contain some other extra points $S = \{s_1, s_2, ..., s_K, K \leq N\}$, called the Steiner Points, resulting in a minimal network, called the Steiner Minimal Tree (SMT). The neural optimization technique of Jayadeva and Bhaumik (1994) is one of the algorithms available in the literature to achieve the SMT. It is difficult to find the exact locations of the Steiner points as size of the point set increases. Jayadeva and Bhaumik have, therefore, added some extra points, called curve points, lying on an open curve, surrounding the given point set. An energy equation is written for the system of the curve points and the given set of points connecting the nearest curve points. Minimizing the energy equation gives the Steiner Minimal Tree. Their technique works fine when the number of points to be connected are small. For larger size problems they have suggested that the problem should be partitioned first into smaller size problems and then their algorithm should be used on the smaller size problems. Finally the partitioned individual solutions are to be concatenated to get the final result. In this work we have found various issues that affect the performance of the algorithm. Solutions to the issues have significantly improved the performance of the algorithm.

DESIGN FOR MANUFACTURABILITY IN ANALOG AND DIGITAL LIBRARY DEVELOPMENT FOR HIGH SEMICONDUCTOR RELIABILITY

Bedanta Choudhury[1]

Abstract

Design for Manufacturability (DFM) is a design methodology for optimizing reliability, yield, cost, quality and time-to-market of integrated circuits, by considering important manufacturing issues pretty early in the design stage. This paper discusses the scope of implementing DFM practices in Analog and Digital Library design. The paper introduces certain basic DFM guidelines and attempts to analyze how these guidelines can be applied to designing some fundamental building blocks of analog and digital circuits, namely standard cells, IO cells, memory leaf cells and PLL. Requirements for manufacturing excellence at times conflict with design-specific requirements. In such cases, implementing DFM practices becomes tough. This paper juxtaposes DFM requirements against design-specific requirements involved in the design of the above-mentioned analog and digital building blocks, and explains how an intelligent compromise can be made through fusion of design expertise with manufacturing process expertise. The paper finally talks about how CAD tools and design flows can be made DFM-intelligent towards realizing higher semiconductor reliability.

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1. Introduction

The evolution of CAD tools over the years has given rise to a great divide between the two paradigms of design and manufacturing of an integrated circuit. There is no doubt that CAD tools have been infusing more and more luxury into the lives of IC designers. But at the same time, rather unfortunately, these tools have been drifting the designers more and more away from physics. But ultimately, it is physics that drives the performance and consequently the economics of the fabricated integrated circuits. Especially in the present submicron era, this divide between design and manufacturing can no longer be afforded. Physics has to be brought back to polygons for manufacturing excellence of integrated circuits.

This is where the concept of design for manufacturability (DFM) steps in. DFM is a methodology of making design decisions during the initial phase of a product design on the basis of a thorough understanding of the technical and economic implications of the fabrication of the product being designed. Clearly

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Impact of Gate to Source/Drain Overlap for Analog CMOS Circuit Application in sub-100nm Technology

C.S.Thakur and N. Bhat[1]

1. Abstract

We report the results of extensive mixed mode simulations to explore the effect of gate to source/drain overlap scaling on analog circuit performance and total gate leakage current. We show that decreasing the overlap length not only decreases edge direct tunneling current, but it also improves the transistor performance metrics such as transconductance, output resistance, intrinsic gain and unity gain transition frequency.

2. Introduction

The aggressive scaling of CMOS devices has been accomplished by decreasing the oxide thickness to obtain high current drive and good control on short channel effect. Several limiting factors associated with the ultra thin gate oxides have been identified, among them, the direct tunneling current is the most sensitive one to the oxide thickness. For conventional CMOS devices, dominant leakage mechanism is mainly due to short channel effects owing to Drain-Induced Barrier Lowering (DIBL). In the sub-100nm technology regime with ultra-thin gate, however, the gate leakage current can contribute significantly to off state leakage. Recent studies have shown that the direct tunneling current appearing between the source-drain extension (SDE) and gate overlap, so-called the Edge Direct Tunneling (EDT), dominates the off-state current [1-3], especially in short channel devices. In this work we have looked at scaling of gate to source/drain overlap length from gate leakage and analog circuit performance perspective. A commercial TCAD software [4] has been used for simulation work.

3. Effect of gate overlap length on total gate leakage current of CMOS device

There are fundamentally two components of direct tunneling current. One is the Edge Component (EC) or Edge Direct Tunneling (EDT, tunneling of carriers between gate and source/drain overlap regions) and another one is Channel

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CROSSTALK NOISE CLOSURE IN DSM DESIGNS

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Abstract

In the DSM era, crosstalk noise analysis and closure presents several challenges. Some of the important issues are predictability in closure, reducing pessimism in analysis, and safe hierarchical analysis and signoff. Often, crosstalk closure is an iterative process involving loops of analysis and fixing, with new violations occurring at the end of each iteration. In this paper, we present a method to achieve predictability in the closure process, by identifying the real and root-cause noise problems that need to be fixed, so that new violations are not discovered after fixing. Identification of crosstalk violations needs to consider the timing information to decide whether a glitch is likely to cause a functional failure. We present a simple method to use the data arrival times and slack information to reduce pessimism in the analysis. A relationship between the timing slack and the glitch criticality is drawn. We discuss the gaps in hierarchical crosstalk analysis methods, and present a flow that addresses the gaps.

1. Introduction

With shrinking geometries in deep submicron designs, interconnect coupling has become dominant. Coupling induces glitches on a quiescent victim net, when there is switching activity on an aggressor net coupled to it. Coupling also affects signal delays when there is an interaction of switching aggressors and switching victims. Crosstalk glitch can cause functional failures, whereas coupling delay is a timing closure problem.

Accurate crosstalk analysis on a design is possible only after detailed routing is complete. Hence, crosstalk noise analysis is performed in the later stages of the design cycle, which poses a two-fold problem: flexibility to perform fixes are minimal, and crosstalk closure becomes a bottleneck in the design cycle. To ensure that crosstalk noise closure is a predictable process, it is essential to identify the real problems, and to minimize iterations of fixing and analysis. At the same time, it is necessary to analyze for the worst-case effects. In this paper we describe a method to identify the set of necessary and sufficient crosstalk fixes required, considering worst-case glitch propagation effects.
The occurrence time of the glitch can be used to check if the glitch will occur in the window of time when the receiving latch cell is sensitive to state changes [4]. We present a new method in which a relationship between glitch violations and the timing slack of the affected receiver is drawn, which can be used to identify and prune false violations. The improvement that our method provides

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Design of High Data Rate Sigma-Delta Analog-to-Digital Converters

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23rd January 2003

Automation of Analog Layout Generation and Design: Parameterized Cell Library Approach

Atul Pandey[1] and Basabi Bhaumik[2]

Abstract

An Analog layout generation tool based on parameterized cell library approach is presented. The tool is designed to generate analog circuit layout, which aims at generating analog circuit layouts that are reusable and retargetable**.**

Keywords: Parameterized cell, SKILL™ , Analog, retargeting, IP.

1. Introduction

The present state of Analog CAD tools makes it difficult to quickly and cost effectively design the new analog circuitry that offsets the time advantage of digital circuit design techniques which has been realized with the advancement of Digital CAD tools. The devices, which are supposed to bring about digital revolution, are surprisingly dependent on core of analog circuitry. Magnetic disk drives, cellular phones and compact disks are such examples. So it becomes imperative to have a methodology compatible to present digital design methods for Analog circuit designs. This method should address the issues of reusability and flexibility.

In this paper, a methodology based on parameterized analog cell library to automate the analog design with the objective of achieving the design specifications has been proposed and demonstrated.

The overview of the methodology is presented in section 2, section 3 focus on parameterized cell library development, section 4 presents the other blocks like netlist converter and device perturbation and router is explained, section 5 presents the experimental result of this methodology on a OTA with conclusion and future scope in section 6.

2. Overview

The efforts for automation of analog building blocks layout is going on for last 15 years but very few strategies has been accepted to be really plausible for generation of large analog blocks. The first such effort was in 1984 when Smith et. al presented their work, which included design of an OTA, based on standard cells. But this library was of little use for general purpose . During late 80's and in 90's lots of efforts were made to automation of analog layout and lots of strategies were developed to tackle the problem.[3],[4],[6] are few of the notable breakthroughs in their respective strategies.

The aim of a layout tool is, given a netlist, specification and design constraints, generate a layout automatically extending the approach for IP design, given a

FRAMEWORK FOR VERIFYING ASSERTIONS USING SEQUENTIAL ATPG

Ravi Kumar. Dasari and Krishna Kumar. D[1]

Abstract

In this paper, we present a framework for verifying the assertions using sequential ATPG (Automatic Test Pattern Generation). The Sugar assertions are mapped into a set of target Fault locations, and by generating the test vector set using Sequential ATPG justifies the status of the property. We also address few procedures to reduce the sequential ATPG effort by considering the type of assertion before they are mapped to target fault sites. Experimental results of verifying the circuits with assertions are presented with the addressed methods.

1. Introduction

As the complexity of the circuits are growing rapidly verification and testing of the correctness of the circuits is gaining more importance. The simulation-based verification process requires typically stimuli for the Circuit model and a simulation monitor, which monitors the correctness of the circuits. Resent progress in simulation has primarily focused on either raising the level of abstraction of simulation or improving the speed of simulation. However simulation based verification has some fundamental drawbacks like generation of good stimuli remains very time consuming and tedious work, and only exhaustive simulation can verify a property. Therefore, it is likely that simulation-based verification will miss some corner case bugs even under long simulation cycles.

Recently significant effort has gone into exploring ways to apply formal techniques to verification. Equivalence checking and model checking are among the more successful techniques for formal verification [1]. Model checking, taking a model of a design and assertions as inputs, determines whether or not the design satisfies the properties. Unlike simulation, the model checking approach searches exhaustively through all the input combinations and the state space. The current model checking search methods can be classified into three categories; namely, explicit methods, symbolic methods, and ATPG based methods. This paper concentrates on sequential ATPG-based approach for verifying the assertions.

Sugar is a formal specification language for hardware. For model checking, the Sugar specification can automatically be translated into one of the standard temporal logics LTL or CTL possibly augmented with auxiliary state machines. For simulation, the Sugar specification can automatically be translated into a simulation checker [2].

Specifying assertions in Sugar and mapping to equivalent fault sites using Stuck at fault model is described in section 3.

2. Background

To understand more details of an assertion-based methodology a common set of definitions is presented.

Property: A general behavioral attribute used to characterize a design. Properties can be high level attributes such as characteristics of incoming and outgoing networking packets or low-level attributes related to the state of a finite state machine.

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COVERAGE – DRIVEN FUNCTIONAL VERIFICATION: TO SPEED VERIFICATION AND ENSURE COMPLETENESS

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Abstract

Functional verification has become a bottleneck in the design process. Functional coverage determines when verification is complete. Verification metrics are a set of numbers used to determine how much design functionality the verification suite has exercised. The quality of verification efforts has become more important than ever because the latest silicon processes are now accompanied by higher re-spin costs. As a result, lengthy design verification has translated into missed market opportunities, while insufficient verification has resulted in higher costs and bugs lurking in released silicon that result in costly problems in the field.

Functional coverage is defined as explicit functional requirements derived from the device and test plan specifications.

This paper suggests an approach of functional coverage, starting from early stages in the verification process. Coverage is used as a goal and as a metric, by which the testbench and test suite will be measured throughout verification process. The approach saves significant human and machine resources, shortens time-to-market and eventually contributes to a mature and timely tape-out decision and a high-quality product.

This paper discusses the need for objective metrics, studies the approaches used before functional coverage evolved and defines functional coverage and the complementary technology. It then demonstrates the proposed approaches using Specman Elite's functional coverage engine. At last, it suggests a flow for maximizing testbench effectiveness.

1. Motivation

Advanced technologies such as design reuse and physical synthesis allow designers to create ever-larger designs. As gate counts exceed one million, verification methodologies have failed to adjust, turning functional verification into the main bottleneck in the design process. Two major challenges are how to reduce the time required for verification to a reasonable size, and how to ensure complete verification.

1.1 Effective Simulation: As exhaustive tests are practically impossible. In order to avoid unnecessary repetitions, the designer should try to answer questions like: Were all possible stimuli variations injected? Were all possible

TEST DATA COMPRESSION FOR SYSTEM-ON-CHIP USING AN ADAPTIVE COMPESSION CODE

Nishant Soni, Santanu Chattopadhyay[1]

Abstract

An adaptive compression algorithm tailor made for compression of test data used in SOC testing is presented. We optimize the compression performance of our algorithm using scan-latch reordering and give experimental confirmation of its superior performance against other algorithms.

1. Introduction

The rapid progress in large-scale integration technology during the last few decades has resulted in larger and larger circuits being crammed into a single piece of silicon. This has resulted in a corresponding increase in the test data needed to test such circuitry, which consequently places a heavy demand on the memory requirements of the Automatic Test Equipment (ATE). The cost of ATE grows in proportion to the increase in the operating frequency, channel capacity and memory requirements of the test data [1], and hence to continue to make the production of chips cost effective it is imperative to reduce testing costs.

One of the ways of reducing the cost of ATE is by compressing the test data before it is stored on the ATE. Reduced volume of test data occupies lesser storage volume on the tester and is also transported faster to the chip. This compressed data is then decompressed using a small on-chip decoder and then applied to the circuit under test (CUT). In this way test data compression is able to relieve the tester of larger storage requirements and at the same time makes the testing process faster . However this method incurs the drawback in terms of the hardware cost involved in constructing the on-chip decoder. The solution lies in compression algorithms which are able to simultaneously satisfy the dual objectives of loss-less compression of test data with minimal decoder circuit area overhead.

Some of the recent works on test data compression algorithms include Golomb [2], FDR (Frequency Directed Run-Length Coding) [3] and VIHC (Variable Input Huffman Coding)[4]. Most of these algorithms are based on encoding only runs of 0's, and hence instead of encoding the actual test data, they encode the corresponding difference vector sequence. Exercising structurally related potential faults in the CUT requires similar test vectors and consequently the

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UNIVERSAL TEST SET FOR DETECTION OF STUCK-AT FAULTS IN GRM (GENERALIZED REED-MULLER) CIRCUITS

Hafizur Rahaman*, Debesh K. Das** and Bhargab B. Bhattacharya***[1]

Abstract: *A GRM (Generalized Reed-Muller) network with EXOR part implemented in a cascade fashion has always a universal stuck-at test set. In [6], a faster design of GRM network is proposed, where all single stuck-at faults can be detected by a test set of length (s+2n+3), whree s = # of product trerm in GRM network in the GRM network [15]. This paper proposes a new design of GRM network that provides a universal test set for stuck-at and stuck-open faults. The proposed design is faster than the GRM network with EXOR part implemented in a cascade fasion. The experimental results also establish the cost effectiveness of our design in comparison to the design presented in [6].*

1. Introduction

With advancement of the VLSI technolgy, economical and highly testable implementations of Boolean functions based on AND-EXOR expression play an important role in logic synthesis and circuit design. Generally AND-EXOR circuit realization of combinational logic suffers from slow speed and larger chip area. However, they are effectively used in design of FPGA-based modules provided by Xilinx, Actel [12]. In many applications, AND-EXOR realizations may occupy lesser chip area than that of the traditional AND-OR synthesis [13]. In addition, these circuits are known to be easily testable. Various design for testability (DFT) techniques for detection of stuck-at faults by a universal test in AND-EXOR circuits are well known [1-8]. Testable realization of RMC circuits for detecting bridging faults with a universal test set was described in [9]. Realizations of these circuits with nMOS are also known to be easily testable [10]. For CMOS implementation of RMC expressions, a robust and universal test set for stuck-open faults was derived in [11]. The technique [14] presented an easily testable CMOS implementation of GRM and ESOP expressions for detecting all single stuck-open faults.

This paper presents an easily testable implementation of GRM expressions for detecting all the single stuck-at faults. Gate-level realization of a GRM expression [6] for detection of the multiple stuck-at faults is implemented as a tree structure instead of a cascade, to reduce circuit delay. However, the test set is dependent on the number of product terms of the functions. The testable implementation of ESOP expressions was presented in [3] for which a universal test set of length (n + 6) exists that detects all single stuck-at faults. This realization is implemented as a cascade structure and the circuit is slower. It has been shown [15] that a test sequenece of length 2n+s+3 is required to detect all single stuck-at fault in the GRM network of [6]. In our proposed scheme, we slightly

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DUAL PROCESSOR MODEL BASED VERIFICATION OF SOC

Kamal Katiyar[1]

Abstract

The foremost concern of a verification environment is to ensure that design functionality matches its specification. It is also used to provide functional stimulus for generation of test patterns for use in post silicon verification. In the latter case the simulation environment needs to be cycle accurate with respect to silicon. However keeping the environment cycle accurate can increase simulation run times to unacceptable limits if software is executed on the simulated environment. The need for cycle accurate environment may also preclude use of present day co-verification tools that help reduce simulation times.

The methodology described here was used to both functionally verify a SoC and also provide the required functional stimulus by reusing the chip level tests. An instruction accurate processor model and a cycle accurate processor model were used in phases of test case development. This enabled cycle time reduction and also kept the tests compatible with cycle accurate environment.

This methodology has been a key factor in eliminating silicon re-spin costs by achieving first pass successes. It has also helped in release to volume production of devices by enabling reuse of functional stimulus for post silicon verification.

Keywords : *Co-Verification, SoC verification, HVL, ATPG*

1. Introduction

Our verification methodology had two aims, first was functional verification and second was to provide functional stimulus for generation of test patterns for screening packaged silicon parts. All test-cases booted up the processor model and executed software which configured and controlled the entire chip. Since the register transfer level (RTL) model of the processor core was not available due to proprietary nature of the IP core, for simulation we used C models. Rest of the design was available as RTL. Next two paragraphs discuss why we needed two different kinds of simulation models of the processor core.

Memory BIST logic may not be present for all memories in the chip, this may be done for saving area or reducing complexity of design. Typically for few small memories, BIST logic may not be added and a simple software algorithm be used to test it through the embedded processor. The designer may also not want to insert scan in certain timing closure sensitive logic like the clock controller.
For our design, described in section 2, the test vectors for silicon were used for IO buffer characterization, for exercising logic with low scan coverage and for screening memories that did not have built in self test (BIST) logic. This meant

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IT IS SUFFICIENT TO TEST 25-PERCENT OF FAULTS

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Abstract – Traditional methods of fault analysis use structural equivalence fault collapsing after the gate-level circuit is flattened. This procedure typically reduces the number of faults to about 50 to 60 percent of all stuck-at faults. Using the recent techniques of functional dominance and hierarchical fault collapsing, we show that the collapsed fault set can be reduced to below 25 percent.

Keywords – Digital testing, fault models, functional dominance fault collapsing, hierarchical fault collapsing, stuck-at faults

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1.0 Introduction

Two faults that have the same tests cannot be distinguished from each other and hence are called *equivalent*. If all tests of one fault detect a second fault, which may have some additional tests, then the second fault dominates the first one. These concepts help reduce the number of faults to be considered in testing via *fault collapsing*.

The prevailing test methodology involves fault collapsing based on structural fault equivalences. For example, for an AND gate all stuck-at-0 faults on the inputs and output are equivalent and just one of those needs to be considered. When applied to large circuits, these local equivalences reduce the number of faults to about 50 to 60 percent of stuck-at faults on all lines (see Bushnell and Agrawal (2000)).

There is another form of fault equivalence, referred to as *functional* or *global*, that specifies equivalence of faults on lines of isolated gates. Such equivalences have been studied in the recent literature. Lioy (1993) shows that functional equivalences can reduce the size of the collapsed fault set of a four-NAND gate exclusive-OR circuit to 10. This circuit has a total of 24 faults and the conventional (structural) collapsing can only reduce the fault set to 16. The analysis of functional equivalences can be expensive and hence can be applied only to very small circuits. An implication analysis, given by Amyeen *et al*. (1999), is efficient but may not guarantee all equivalences. The hierarchical collapsing method of Prasad *et al*. (2002) allows the functional equivalences of small cells to be used for fault collapsing of very large circuits. They show that the collapsed set of an 8-bit adder circuit designed with exclusive-OR cells reduced to 38-percent when functional equivalence and dominance collapsing is

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Test Cost Computation and Reduction Techniques

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Abstract

The problem of testing VLSI designs is becoming more complex with newer process technologies. These technologies allow much more number of transistors to be packed into the die, which results in correspondingly more logic to be tested on a device. Also, these technologies exhibit newer failure mechanisms, which require the application of specific tests which were hitherto unnecessary. Some of these tests also require the use of expensive testers for their application. Also, based on the device package and the test conditions, the test infrastructure (boards, probes) required is more sophisticated. These factors are contributing to the increasing cost of testing modern VLSI devices.

The cost of testing a device has a direct impact on the profitability of the device. Test costs are incurred in terms of the additional design effort, the test automation required, the area required to implement DFT features, the overall test and tester infrastructure, and the time spent on the tester for testing the device.

REDCUED PIN COUNT TESTING USING IEEE 1149.1 ENVIRONMENT

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Abstract

Reduced Pin Count Testing (RPCT) provides an effective manufacturing test methodology such that packaged devices with large numbers of pins can be tested using relatively low cost testers. This can be achieved by reducing the number of pins that come in contact with a tester during execution of structural test for the device. In other words, the device can be tested using a low-cost tester with few full-functional channel pins (AC pins) when compared to the total number of signal I/O pins in the device itself. In RPCT, the IC pins associated with power and ground, scan I/Os, clocks, control signals, and possibly some analog signals come in direct contact with the tester, while all the remaining functional pins are accessed via the boundary scan chain. The effect of RPCT is maximized only when there are a small number of pins that come in direct contact with the tester.

This can largely impact the tester-cost savings, as the number of tester pins almost directly controls the price of a logic tester. Moreover, with ever-increasing device pin numbers, such a technique could increase the test-floor throughput thereby preventing under-utilization of existing testers.

Another advantage that stems out from this technique is the ability to use the TAP controller for generating sequential patterns requiring pulsing the one (or more) system clocks in the capture cycle. This can be accomplished by placing the TAP controller in the idle state and transferring the control of the clocks to the tester that is applying the test vectors.

There is no significant drop in coverage metrics observed in the number of ATPG patterns created for the design and essentially the same number of test patterns is needed for both the traditional scan based testing and reduced pin count testing methodology.

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Genetic Algorithmic Technique for Integrated Testing of Cores and Interconnects in SOC

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Abstract

This paper proposes a solution for the integrated testing of cores and the interconnections between them in System-on-Chips(SOCs), targeting to reduce the test application time. To date, various studies have focused only on the problem of testing the cores and not much literature exists on the testing of interconnections. Reducing the core-testing-time and the interconnection-testing time individually does not yield an overall reduction in the testing time. Our genetic algorithm based approach minimizes the overall testing time, reducing it significantly as compared to that obtained by reducing the core-testing and the interconnection-testing times separately.

1 Introduction

Design of large System-on-chips using embedded cores has become a common practice today. The increased use of cores has made the testing problem very difficult. The testing procedure involves the testing of the cores and the interconnects between them. Testing time can be minimized by the design of efficient TAM architectures, optimization of core wrappers, and test scheduling. Most of the prior works have addressed the problem of minimizing the core testing time [2,5] and have ignored the testing of interconnects, which in some cases may have a major share in the overall testing time, particularly if the density of interconnections between the cores is high. The problem of *partitioning* of the total TAM width among the given number of TAMs, an *assignment* of cores to TAMs, and the wrapper design for each core to minimize the testing time, was addressed in [2]. It solved the problem optimally using Integer Linear Programming. However ILP is in itself an NP-hard problem, and execution time can be quite high for large SOCs. In [1], the GA based approach has been used to solve the problem. The problem that we address in this paper is as follows.

Determine (1) a partition of the total TAM width among the given number of TAMs, (2) an assignment of cores to TAMs, (3) a wrapper design for each core, and (4) scheduling for testing of interconnects, such that the overall testing time is minimized.

We solve this NP-complete problem using Genetic Algorithm. We have chosen TESTRAIL [3] as the TAM architecture. Since the present benchmark circuits do not contain any information about the interconnections, we have used a pseudorandom number generator to generate the interconnections of varying

A study of Parallel test application for core-based SoC designs

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Estimating the Fault Coverage of SOCs Using Module Coverage Data

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Abstract

An SOC (system-on-chip) consists of a collection of several pre-designed modules integrated together to realise the particular system. Obtaining the fault coverage of the SOC using conventional ATPG (automatic test pattern generation) techniques is possible only when a fully integrated netlist is available. As the modules are already pre-designed, it is almost too late to recover any coverage loss by incorporating additional DFT (design for testability) techniques. On the other hand, an accurate estimation of the device (SOC) fault coverage, based on module level coverage data, will help to address this problem. The coverage data for the individual modules can be used to estimate the device coverage, as well as to quantify the impact of the loss of coverage in a particular module at the device level. The modules with high impact can be modified early to improve the coverage

This presentation describes techniques for such an estimation. Its main contributions are the development of a simple framework for obtaining the upper and lower bounds on the device coverage, and techniques for more accurate estimation of such coverage within these bounds. In the process, it also identifies design considerations to enable the device coverage to be as close to the upper bound as possible. Experimental results are presented to illustrate the usefulness of this approach, as well as the limitations in the estimation process.

Estimation of Test Power in Embedded Memories

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Detection & Analysis of Faults of CMOS Op-Amp

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In this paper, the analysis of faults in analog MOS blocks, including the testing and testability, is pursued. Using a two-stage compensated Op-Amp, the catastrophic and parametric faults are analysed. The limitations on the number of nodes, at which measurements of voltages and signals in an integrated MOS block can be done, imposes severe limitations on the fault detection of analog circuits. Using the DC analysis of voltages at the output node and the DC current measurement at the power supply, detection of catastrophic faults is analysed. Also, depending upon the tolerance of the fabrication process, the relation between the parametric fault and usability of the circuit is studied. In our case, simulation results show that the circuit suffering from catastrophic fault is highly unlikely to behave as a fault free circuit due to its cancellation by parametric faults.

Index terms: IDDQ testing, testing and testability of Analog MOS blocks, integrated circuits, two-stage compensated Op-Amp, pseudo power factor, Monte Carlo analysis, DC analysis, catastrophic fault, parametric fault.

1. INTRODUCTION:

Analog integrated circuits are widely used in many applications but there remain considerable difficulties in testing of these circuits. These difficulties include the nature of signals involved and the diversity of specifications to be checked in order to assess the correctness of the circuit. In addition to these constraints, problems include parasitic capacitances and limited accessibility to the internal nodes of the IC. As the fabrication process cannot be stalled for testing of correctness, the nodes at which measurements can be performed are only the nodes available for output. Moreover, the actual size of the transistors fabricated into silicon has certain variance due to process variations. This increases the challenges in testing of analog integrated circuits. There are several statistical models proposed to detect faults with certain probability associated with it [1][2][3][7]. However, to detect whether the circuits are faulty or not doesn't throw any light on the cause of the fault: Catastrophic or Parametric and the point of failure. The idea of IDDQ [10][11] like testing of analog circuit is borrowed from the digital domain analysis for fault detection of digital circuits. Using the DC analysis along with the measurement of the bias current drawn from the supply, it is possible to determine faults, deterministically, at certain nodes. Using a two-stage compensated Op-Amp, we tried to pinpoint the node at which the circuit has failed due to catastrophic fault. It should be made clear at this point that numbers mentioned in Fig 2 near the nodes are node numbers and