Tackling Signal Integrity Issues during DSM Design

B Anantha Bhat[*]

The marked increase in the contribution of interconnect delays to the overall path delay in deep submicron VLSI circuits is well noted. The consequent *timing closure* problem between front end and backend stages of design can result in several design iterations and wreck project schedules. This is addressed by unifying synthesis and placement.

The very same physical effects are resulting in one other major shift. Signal capacitances can be split into two parts:

- Capacitance to substrate
- Capacitance to adjacent geometries (Coupled Capacitances)

It is seen that latter component dominates over the former with shrinking silicon geometries. This impacts many aspects of the design, the most critical of these being the design timing. While parasitic extraction technologies have matured to extract these coupling capacitances, there is an urgent need to upgrade the static timing analysis methodologies to take into consideration the effect of coupling capacitance on timing.

The proposed presentation touches upon how this impact is essentially a dynamic phenomenon, but can be analyzed through *Static Cross talk analysis*. It discusses issues involved in such an analysis.

Some of the other challenges in ensuring design integrity in DSM are

1) Voltage Drop analysis (to prevent performance degradation)
2) Current Density Analysis (to avoid Electromigration problems)

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AN EXTENDED MEMORY ARCHITECTURE FOR REAL TIME MORPHOLOGICAL SIGNAL PROCESSING

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Abstract

Mathematical morphology is a shape-based approach to process signals such as images. The main applications of mathematical morphology are image segmentation, smoothing, filtering, medical imaging, pattern analysis, machine vision, surveillance, etc. With the advent of new video compression standards like MPEG 4 and MPEG 7, video segmentation has attained great importance. Video segmentation is a process of decomposing video sequences into moving objects and background. Morphological based segmentation techniques are quite popular in effecting object segmentation on individual frame basis. However, to perform these operations in real time, is a challenging task owing to the computational complexity. Morphological operations such as opening, closing, thinning, region filling, etc. are obtained iteratively by using basic building blocks, dilation and erosion. These are non-linear mathematical operations, which are computed using a coefficient matrix called the structuring element. Computational complexity varies proportionately with the size of the structuring element. In addition to the computational complexity, morphological operations such as thinning, thickening, etc. require 4x(MxN) bytes of memory for implementation, where MxN is the size of the processed image. If these operations are realized on a DSP, the processing time will be high since the instructions are executed sequentially.

This paper proposes an extended memory architecture to perform morphological operations in real time. This architecture is suitable for ASIC implementation owing to a high level of pipelining, parallelism and regularity of the structure inherent in the design. The memory utilization in this architecture is only 2x(MxN) + 4xN, which is nearly 50% of the memory requirement mentioned earlier. The processing speed of this design implemented on ASIC is likely to be over five times that of the implementation on TMS320C6201 DSP for the same operating frequency.

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TEST AND INTEROPERABILITY OF AN OPTICAL SIGNAL PROCESSOR USING THE CONCEPT OF TRANSFORMS

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ABSTRACT

Definition of an Optical Signal Processor

The Optical Signal Processor is also reconfigurable and can be dynamically tailored to the required transform type. Unlike hardwired ASICs or reconfigurable FPGAs, it provides on-the-fly programmability, flexibility and upgradeability. The performance of such processors is quite independent of the type of transform being used. The processor could be made to be available as an off-the-shelf module with a roadmap indicating where it can be embedded in DSP cores, ASSPs (Application Specific Standard Products) and Systems-On-a-Chip. One more important advantage of an optical processor is that it allows software designers to work at a much higher level of abstraction. This is because the device executes transforms instead of the ordinary MACs in the case of DSPs. Instead of handling algorithms at individual data points, algorithms for handling the entire vector could be processed, shortening the computational complexity and speeding the time-to-market for new products.

Test and interoperability with a DSP Controller

The test setup with the OSP achieves interfacing with a TMS320C24x™ DSP controller and is used to demonstrate signal conditioning of a simulated network. The system code of the OSP is executed out of Flash at 110-120 MIPS while time-critical code requiring 150 MIPS of performance is executed directly out of the 18kW of the on-chip RAM of the DSP. This is something different in the OSP architecture from normal DSPs. In addition, the DSP offer an external memory interface with an address reach to incorporate the “optical memory” model of the OSP. The OSP communicates effectively through optimized event managers that include flexible pulse-width modulation (PWM) generators, programmable general-purpose timers and glueless capture and encoder interfaces. Multiple standard communication ports provide simple communications interfaces to the host and the interface I/O devices. The OSP has an in-built Control Area Network (CAN) controller that provides an interface to the DSP. As the DSP used has a CAN controller as well that provides an interface to backplane applications, it is attempted to synchronize

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Memory Exploration for Embedded Systems

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Abstract

The memory architecture of an embedded system strongly influences its cost, power, and real-time performance. Memory is organized hierarchically and includes on-chip SRAM, data and instruction caches, and off-chip memory, which is a combination of ROM, SRAM, DRAM or flash memory. On-chip memory is organized into multiple banks with one or more ports per bank. The access time and cost of the each memory type is different, posing conflicting requirements in optimizing the overall cost and performance.

Designers can take advantage of the application-specific nature of embedded systems to optimize the memory subsystem architecture. The memory access characteristics of the applications are analyzed a priori using profilers. An example is the code and data layout optimization, where the code and data sections of the application are intelligently placed so as to minimize the number of CPU stalls. Similarly, the problem of finding the optimum memory organization (types of memory, number of memory banks and single/multi port memory) can also take advantage of the memory access characteristics of the system. This paper will study the various aspects of memory exploration for embedded systems and survey the existing literature on the topic.

1 Introduction

Embedded systems consist of one or more embedded microcontrollers, digital signal processors, application-specific circuits and read-only memory, integrated into a single system-on-chip (SOC) package. See Figure 1. Since they are customized to run specific applications, the application software is preloaded in the read-only memory. Application areas where embedded systems have made significant impact include cell phones, videophones, automobiles, and industrial automation. Since embedded systems are commodity products and are sold in high volumes, their design is primarily driven by market cost. Power consumption and real-time performance are other key design considerations.

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CNB02: Bluetooth™ SoC

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Abstract

With the electronics circuits shrinking, designers are putting more functions into single chip. Imagine having a Bluetooth™ controller complete with integrated processor, memory, radio, and baseband controller with added interface of GPIO, USB, SPI and UART. Take this chip and you can develop complete Bluetooth™ enabled device with minimum parts very quickly. CNB02 is an Integrated Bluetooth™ Controller SoC. It's a single-chip Bluetooth™ Radio Transceiver, baseband controller with 8KB memory, an integrated 32 bit processor with 2KB Cache and 64KB embedded SRAM. The ASIC includes peripherals such as UART, USB, SPI, GPIO, and CVSD Transcoder. This paper presents the issues related the SoC activities.

1. The Chip

The CNB02 is a single-chip Bluetooth Radio Transceiver and Baseband Controller with an integrated 32 bit RISC microprocessor and 64kB of embedded SRAM.. A fully integrated frequency-hopping RF transceiver requires only an external matching network and antenna to build a Class 2 or Class 3 radio. The programmable transmit power attenuator enables Class 1 operation with an external fixed gain Power Amp. Host interfaces are provided via two fast (921kbps) serial ports and a USB 1.0 engine, which can be operated in either host or device mode with the appropriate firmware. A CVSD Transcoder supports Bluetooth voice applications.

1.1 Specifications

- V1.1 Blue-tooth Base band Controller + Radio
- 2.4GHz Frequency-hopping radio with +4dBm Power Amp & 20dB TX
- Attenuator
- 32-bit RISC processor with 2kB Cache
- 64kB on-chip SRAM
- CVSD Transcoder with PCM and 16b linear CODEC Interfaces
- USB 1.0 Engine with Host and Device modes
- Two fast UARTs, 921kbps each
- 1.8V, 40mA Power Consumption (typical)
- 128 pin LQFP (14mm x 14mm)
- Operating Voltage 3.3V/1.8V
- TSMC 0.18u RF CMOS Process
- Die Size: 5mmX5mm

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Integrated Design Of An Image Processor Using DSP And ASIC Cores

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Although digital signal processors (DSPs) are suitable for filters and multiply and accumulate (MAC) intensive operations, they may not be suitable for video processing applications, since they have limited pipelining and parallelism inherent in their architecture. Further, multimedia-specific instructions cannot be effectively incorporated in these processors because it is difficult for compilers to predict when they may be used. In contrast to this, FPGA/ASIC implementations exploit massively parallel and highly pipelined architecture resulting in high-speed performance, which cannot be matched by DSPs. However, DSPs have very efficient ways of handling data transfers with external peripherals. On the other hand, hardware logic based on ASIC/FPGAs takes a long time to design and build, while providing little flexibility for future adaptation. The present work is an attempt to combine various features mentioned earlier on a single core offering the high performance of the ASIC and the flexibility of DSPs.

We illustrate the above design methodology by integrating a synthesizable, general purpose I/O processor along with DMA feature and DCT/IDCT core as image processing co-processor for a high performance programmable DSP. In this method, only those new processing modules that need to be integrated are designed, leaving the already existing features untouched. Various issues such as speed, image size etc. have been analyzed to validate the use of this design for image processing. Image processing application has been considered only to illustrate the working of the proposed design methodology. This methodology can be easily adapted to any other application.

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A Simple Delay-Testable Design of Digital Summation Threshold Logic (DSTL) Array

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Abstract

A new cellular array is introduced for synthesizing totally symmetric Boolean functions. The cellular structure is simple and universal – it uses only 3-input, 3-output AND-OR cells, and admits complete path-delay fault testability. The design is an improved version of the classical DSTL array reported earlier by Hurst [1], that eliminates path-delay untestability of the earlier design. The new design also admits a universal test set of length 2n that detects all single stuck-at faults, where n is the number of input variables. The proposed design is useful in view of the fact that two-level realizations of most of the symmetric functions are known to be path-delay untestable.

1. Introduction

In this paper, we introduce a cellular logic array similar to *digital summation threshold logic* (DSTL) reported earlier by Hurst [1] in connection to synthesis of threshold logic. Such an array can be used directly for synthesizing unate symmetric functions. Non-unate symmetric functions can then be synthesized by the method proposed in [4]. A testable logic design using DSTL arrays for detecting stuck-at and bridging faults appeared earlier in [5].

One major drawback of the classical DSTL array is that it is not completely delay testable. The hardware and speed of the proposed design are same as that of [1] and at the same time our design is 100% path-delay testable. The proposed design consists of an iterative arrangement of identical cells, each consisting of three inputs and three outputs.

As in [1], our design approach is universal, i.e., it depends only on the number of variables, n. The proposed modification can be used to synthesize any arbitrary symmetric function that are 100% path-delay fault testable.

For stuck-at faults, our design admits a universal test set of length 2n, where n is the number of variables.

2. Preliminaries

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WIRELESS LAN MAC (802.11 MAC) FROM CIPL

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Abstract

This paper describes the problems and the challenges that are faced in developing ControlNet India's IEEE 802.11 compliant Media Access Controller (henceforth referred to as 'the MAC'). The MAC is aimed to be an easy to integrate IP core. This means that it should be readily usable for the design houses that develop IEEE 802.11 compliant hardware devices. This demands that the architecture should be as modular as possible. All the external and internal interfaces are required to be very generic in nature. The MAC has interfaces with a base band processor (henceforth referred to as 'PHY', the physical layer comprising of RF plus BBP). the host CPU and an external processor as shown in fig 1.1 below. Thus there is a software as well as firmware that are talking to the hardware. This paper highlights some of the problems faced and their resolves in meeting the required specifications.

Keywords:

IEEE 802.11, 802.11a, 802.11b, Media Access Controller, MAC, PHY, Wireless, LAN, Intellectual Property (IP), Direct Memory Access (DMA), Firmware

1. Introduction

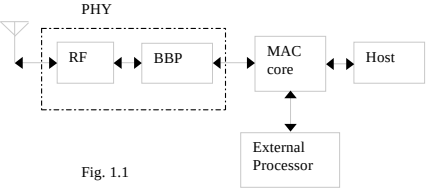

Fig. 1.1

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Design of a Generic CELP Architecture

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Abstract

Modern mobile communications require optimum bandwidth utilization with minimum loss, delay and good quality of speech transmission. This triggered the usage of low bit rate voice Codecs among which CELP Codecs inherit the merits of both Waveform and Source codecs, like toll quality, low bit rate etc. In this paper an attempt has been made to form some special generic hardware blocks for the ITU G.729 standard (CS-ACELP, Conjugate Structure Algebraic Code Excited Linear Prediction) of 8Kbps bit rate CELP algorithm. This is aimed at overcoming the limitation of computational burden and also scaling this application for enhanced speed and large number of channels.

Keywords: CS-ACELP, DSP, Parallelism, and Pipelining

1. Introduction

Up to now we have seen most of the speech codecs [1] are implemented in general purpose programmable DSP, which supports only few numbers of channels. Among the present day codecs., CELP codecs [2] can achieve high-speech quality at extremely low bit rates. But the formidable computational complexity limits it from supporting more numbers of channels with the programmable DSP.

This motivates the IC designers in developing the hardware accelerators or HW-SW co-design methods In this paper, G.729 (CS-ACELP) ITU-T [3] standard is taken as reference. The G.729 CS-ACELP [4] algorithm is used today in applications requiring high quality speech compression such as Video Conferencing, VON (including VoIP, VoDSL, VToA), Digital Satellite Systems, Digital Mobile Radios (specially for Military use), PSTN, and ISDN. Yet, as exemplified by G.729, as compression ratios, algorithmic delay and the subjective quality of speech compression algorithms improve, the complexity of real-time implementation generally increases. It is only with the advent of high performance, low cost DSPs that this implementation can be realized in practical systems. Furthermore, optimized assembly language programming today remains the only viable route to a cost effective single chip realization of a full-

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ICie : Image Compression through Integrated Effort

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Abstract

There is a new generation of digital signal processors for image and video compression and decompression. Regardless of their complexity, most of the image and video compression architectures share three major components, an accelerator for computing two dimensional Discrete Cosine Transforms (DCT) and Inverse Discrete Cosine Transforms (IDCT), a Motion Estimator and a Variable Length Coder/Decoder. This paper documents the maiden effort of twenty one students, from three different colleges in designing "ICie": Image Compression through integrated effort, the design of a 2D-IDCT, Complementary Metal Oxide Semiconductor (CMOS), Very Large Scale Integration (VLSI) architecture based upon block-by-block implementation, in a decoder unit of an image compression integrated circuit(IC). The processor operates on 8x8 blocks of data. Inputs include the DCT values of an image per block at a time, and external control signals. Input values have a wordlength of 15 -bits for the IDCT.

1. INTRODUCTION

Discrete Cosine transform (DCT) is generally recognized as the best transform method to compress the digital picture information. DCT has been widely used in the implementation of low rate codecs for video compression. DCT has become an integral part of several standards such as Joint Photographic Experts Group(JPEG), Motion Picture Experts Group(MPEG), CCITT. Initially, the idea was to implement both the DCT and the IDCT blocks to come up with a comprehensive chip, that would work. But as we proceeded, we exceedingly realized that due to the time crunch we were facing, this was not a possible proposition. So, we decided to pursue the IDCT block alone, as it is more commercially viable.

This paper is organized as follows: The 2D-IDCT and relevant properties are briefly discussed in section 2. The algorithm to be implemented is presented in section 3. The architecture incorporating our algorithm is described in section 4. Section 5 talks about the Simulation for wordlength and Signal to Noise Ratio (SNR) calculation. Data translation and integration issues is discussed in section 6.

2. 2D-IDCT

DCT transforms data into a format that can be easily compressed and hence this characteristic of DCT makes it ideally suited for image compression algorithms. These algorithms help to minimize the amount of data needed to recreate a digitized image. A straight forward implementation of the

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Design of an Embedded Microprocessor and its FPGA Implementation

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ABSTRACT

An embedded microprocessor: an 8085 prototype with I/O ports, was custom-designed without relying on IP blocks. Of special mention is the design of the control unit. The modular design of the control unit enables us to easily extend the instruction set or replace the instruction set altogether. The control unit is partitioned into the flow controller and the control logic. The flow controller decides the next state depending on the instruction fetched and the status of the various flags. The control logic sends the appropriate control signals depending on the current state and the group code. Presently the control unit can support 180 opcodes in the 8085 instruction set.

The design was entered in VHDL, mapped to Xilinx Virtex-E FPGA Technology (using Synplify Pro), and optimized for timing constraints. It was finally taken to a Xilinx place and route tool to give the final product.

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DESIGN, SIMULATION AND SYNTHESIS OF FUZZY CONTROLLER USING VHDL

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Abstract

Growth in the number of fuzzy logic applications has fuelled the need for computing systems with a generalized architecture that efficiently process fuzzy inferences of different applications. Although software solutions exist, hardware structure supports systems to achieve adequate processing speeds for applications from real time controllers to complex expert systems. The use of fuzzy technologies in real -time control problems demands the development of new processing structures, which allow efficient hardware implementation of inference mechanisms. This paper deals with the simulation and synthesis of generalize d fuzzy controller architecture.

The fuzzy controller architecture designed consists of three modules, the fuzzification block, the rule inference block and the de - fuzzification block. The real time crisp inputs are given to the fuzzifier block. The fuzz ified values are manipulated as per the rules stated in the rule inference block. The output of the rule inference is fed to the defuzzifier block, which gives real time control signals. The user can set crisp inputs and outputs, membership functions and th e rule inferences depending on the application. Two architectures, one with triangular overlapping membership functions and another with rectangular non -overlapping membership functions are designed. The two architectures are simulated using View - Logic tools and one of the architecture has been implemented in Xilinx XC 4025 using Xilinx synthesis tools.

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CARAPACE: VIRUS RESISTANT COMPUTER ARCHITECTURE

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Abstract

Computer viruses pose an increasing risk to computer data integrity. They may compromise existing data files or make executable files unusable. Present solutions against viruses are embodied only in software. As the problem of viruses increases, we need tools to detect them and to eradicate them from our systems. The focus is on viruses that affect application executables. We have analyzed the existing software methods for virus detection and have devised an architecture, which uses these techniques in order to detect viruses. Another approach to a virus resistant architecture has also been proposed. The second architecture tries to analyze the instruction mix of the existing viruses and uses the approach utilized by dynamic heuristic scanners. We are currently trying to simulate the effectiveness of the architectures in virus detection.

Keywords: Virus, Tailpatching, Overwriting, Routine replacement, Architecture, Pattern matching, Virus heuristics

1. Introduction

Traditional methods of a hardware-based approach to virus resistance are very trivial. One method advocates the use of locks on floppy disk drives. Other approaches prevent infection and do not behave as 'detectors'. We concentrate on viruses that affect application executables. We shall explain the modus operandi of these viruses.

1.1 Modus Operandi:

In order to investigate how a virus affects and executable file we shall first discuss the general format of an application executable. In simple terms, an application executable (AE) is just a sequence of instructions whose execution is done when the AE is executed. It consists of a segment table and a series of code segments. These segments need not always be stored sequentially. A detailed explanation is provided in [3],[5],[6],[7].

There are 3 ways by which a virus can affect executables

(1) **Tailpatching**: By this technique extension of the segment table takes place to allow the inclusion of an additional entry for the viral code. As

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EMBEDDED RISC PROCESSOR AIMED AT WIRELESS APPLICATIONS

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Abstract

This paper proposes the design methodology of a 32-bit RISC processor aimed at wireless and embedded applications. The embedded domain has had an all-pervasive effect in the recent past. In order to sail with the tides, the designer is forced to add more complex functions into the chip. The protocol side of designs has seen emerging interest in the 802.11x and Bluetooth. In order to enhance this ubiquitous connectivity, we build a processor that supports the above protocols. The instruction set architecture has two parts. A 32-bit component, which is proposed to be an extended version of the original ISA to cater for wireless applications and the other 16-bit component specifically aimed to meet embedded application requirements. While the former application demands powerful instruction implementation, the latter requires high code density.

The basic feature of the architecture is a 3-stage instruction pipeline, comprised of Fetch, Decode and Execute stages. The memory organisation is Von Neumann with load-store architecture, optimizing data processing instructions. An intelligent on-chip bus structure, which is pipelined in nature, enhances system-on-chip implementation. Special emphasis has been given to hardware-software partitioning, to decide upon the level of hardware support for enabling 802.11 and Bluetooth. A comparative study is made on the impact of these protocols on the processor architecture.

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WALLACE TREE SQUARER FOR DSP APPLICATIONS

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Abstract

Datapath elements play significant role in Digital Signal Processing (DSP) applications. Squarer elements assume applications in computing squared error norm (which is minimized in many DSP algorithms to find filter parameters), to compute energy of signal/power spectrum, used in Kalman filter which uses squared values in real time, and applications can also be extended to image processing. So there is a need to design squarer with high performance and high throughput.

In this paper, the implementation of an efficient Wallace tree squarer architecture is presented. Wallace tree architecture compresses the number of signals to be added at each stage resulting in reduced delay. For an n bit squarer, with $p:q$ *compressor, the delay is proportional to* $\log_{\frac{p}{q}}(n)$.

Comparison is made between Wallace tree multiplier, and Wallace tree squarer in terms of speed, area and power. The synthesis was performed using Synopsys DC using the Verilog HDL, and the physical design was carried out using Avant!, Cadence and Magma tool set. The implementation was done in 0.13µ CMOS, 6-metal, 1.2V technology and the Squarer typical critical timing path is 2.5 ns. The resultant area shrink for the Squarer is 15%.

1. Introduction

Squarer is a multiplication in which multiplier equals multiplicand. When the multiplier is used as squarer, the power consumption will be more. Any extra logic added, to operate the multiplier as squarer claims area overhead. Also many DSP applications need to implement a squarer design. In this paper, the implementation of an efficient Wallace tree squarer architecture is presented and is compared with Wallace tree multiplier.

The architecture of the Wallace tree was discussed in section 2, and the implementation details were presented in section 3. Section 4 shows the results of the Wallace tree Squarer and Multiplier and section 5 summarizes with applications to DSP and the future strategies.

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Computer Aided Fuzzy System Design and Simulation

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Abstract

Recently, fuzzy systems are becoming popular largely due to their success in several consumer products such as washing machines, camcoders, cameras, automotives etc. The systems based on fuzzy logic concepts have advantages of simplicity of design and ease of implementation. Several tools have been developed in order to facilitate the fuzzy system design and simulation. For a successful design, simulation and implementation of a product which incorporates fuzzy system, a tool which gives an user-friendly, easy to learn, useful features, powerful design and simulation capabilities, good user manuals will become very attractive. We carry out a review of the tools for fuzzy system design and simulation in this paper. A comparative study of fuzzy system tools is also carried out. The fuzzy system design for Mobile phones is used as a case study. We present the simulation results along with the implementation details for the fuzzy system case study.

1.0 Introduction

It has been more than 30 years since the concept of fuzzy sets was introduced by Lotfi Zadeh[1]. Then came the design of the controllers based on the fuzzy sets concept by Mamdani et al. Several consumer products incorporating fuzzy logic controllers, such as washing machines, camcoders, TVs, etc have hit the market in the past decade. Fuzzy logic has thus become very important technology.

The products incorporating fuzzy logic have been termed to have “High Machine IQ”, since they operate on the principles similar to Human like reasoning. The fuzzy logic applications range from finance/ defence/ automotive/ consumer electronics/ space/ aircraft/ and many more.

For easing the fuzzy system design, a number of tools, both commercial and academic have been developed. Most of the currently available tools have been reviewed in this paper. This paper is organized as follows: In the next section, a brief introduction to the fuzzy sets and fuzzy systems is provided. In section 3, we

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Hardware Designs For Video Compression Algorithms

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Image processing applications such as high definition television, video conferencing, computer communication, etc. require large storage and high speed channels for handling huge volumes of data. In order to reduce the storage and communication channel bandwidth requirements to manageable levels, data compression techniques are imperative. Data compression of the order of 20 to 50 is normally feasible depending upon the actual picture content and the techniques adopted for bringing about the compression. Although software implementations are easy to realize on general-purpose microprocessors, multi-processors or digital signal processors (DSPs), their instruction sets are not well suited for fast processing of high resolution moving pictures. In addition, the instructions are executed sequentially, thus slowing down the processing further. In contrast to this, hardware implementations based on FPGAs and ASICs can exploit pipelined and massively parallel processing, resulting in faster and cost-effective designs. Over the years, several implementation schemes have been proposed to realize various building blocks of the encoder and decoder for processing of still images and motion pictures. These developments have been made possible partly due to ingenious algorithms and partly due to the rapid technological advances made in the recent past in the area of VLSI. This presentation will highlight some of the recent designs carried out in our laboratory for image and video compression applications using DCT and DWT-based algorithms.

A dynamically reconfigurable video encoder to switch among many different applications is designed. The scheme is suitable for FPGA/ASIC implementation and conforms to JPEG, MPEG-1, MPEG-2, and H.263 standards. The design incorporates several novel ideas and algorithms such as controlling image quality on the fly. As a result of this new feature, which uses a concept called pruning, the processing speed increases by a factor of two when compared to the conventional method of processing without pruning. The design also integrates a new, fast, one step search algorithm for motion estimation in video sequences. The design has been realized by using HDL codes. The FPGA implementation is capable of processing color pictures of sizes of up to 1024 x 768 pixels at the real time rate of 25 frames/second.

Although digital signal processors (DSPs) are suitable for filters and multiply and accumulate (MAC) intensive operations, they are not suitable for high resolution video processing applications. In contrast to this, FPGA/ASIC

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Minimum Dynamic Power Design of CMOS Circuits by Linear Program Using a Reduced Constraint Set

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Abstract

The minimum dynamic power consumption occurs in a CMOS circuit when the delay of each gate exceeds the differential path delay at the gate input. Such a design can be obtained by a linear program (LP) that determines the gate delays under a set of path delay constraints. These constraints specify the minimum energy conditions for all gates and the overall input to output delay requirement for the circuit. The LP then finds a solution with minimum number of delay buffers. In this paper, we derive a new LP constraint set. The size of the constraint set, generally exponential in the circuit size when path enumeration is used, is reduced to a linear complexity. This constraint set is obtained by introducing two new (minimum and maximum) arrival time variables at every gate, besides the inertial delay of the gate. These constraints guarantee the same proven minimality of the dynamic power as the path delay constraints. The LP solver in the AMPL package produced identical results for several circuits. This model can also be used for the acceleration of critical paths in a circuit. As an example, the circuit c880, which has 469 gates, required 3,611 constraints in comparison to the 6.95 million constraints needed for the path delay method.

1 Introduction

The topic of this paper is the reduction of *dynamic power* consumption of digital CMOS circuits. When an input vector is applied to the combinational logic, the minimum requirement for each gate is to produce either one or no output transition. However, in reality they produce many transitions. These extra transitions are caused by the differential delays of paths leading to the inputs of gates. This subject is widely discussed in recent books [3, 5, 9–11]. Among various methods for minimizing the dynamic power is the *balanced delay* method in which we equalize the delays of all paths incident on a gate. The advantage of this method is that delays are only added to fast paths, and so the overall delay of the circuit need not increase. However, when a signal fans out, its delay affects several paths and balancing may require insertion of delay buffers on selected fanout branches. Since the buffers consume power, the balanced delay method also adds to power consumption.

An alternative to balanced delay method is the *hazard filtering* technique [1]. In this method, the transients that would have been produced at a gate output due to arrival of signals at its inputs through differential path delays are eliminated by increasing the inertial delay of the gate. Clearly, the overall delay of the circuit will increase.

It is possible to combine delay balancing and hazard filtering to obtain the minimum energy design under the given overall circuit delay constraint. This is done by a linear program (LP) [2, 4]. Though the method leads to a provably minimum energy design, the constraint set of LP becomes exponential in the number of gates in the circuit. This is because, to write these constraints for a gate, all paths between the gate and primary inputs must be enumerated. In addition, all paths between primary inputs and primary outputs must be enumerated to hold the overall delay of the circuit within the specified limit.

The contribution of this paper is to reduce the number of constraints for the LP to a set whose size is linear in the number of gates. This is done by defining two new variables for each gate, besides its own inertial delay. The new variables are the maximum and minimum arrival times, respectively, at the output of the gate. This set of three variables per gate allows us to write the constraints for the gate locally, in terms of its own variables and those of the fanin gates. In Section 5, we prove that the reduced set of constraints still guarantees the *minimum transient energy* (MTE) design with lowest possible dynamic power dissipation.

A COMPARATIVE ANALYSIS OF FLIP-FLOP ARCHITECTURES FOR LOW-POWER USING POWERSIM

Jwalant Joshipura[1]
Pankaj Rohilla
Bipin-bandhu Malhan
Shubhyant Chaturvedi

Abstract

*A user-interactive utility tool "**Powersim**", designed for performing a comparative analysis on low-power flip-flops, is introduced. The paper begins with a brief introduction, emphasizing on the significant contribution of flip-flops towards power dissipation in digital design. Five well-known and published low-power static flip-flop architectures have been designed following certain essential guidelines for low-power. An architectural description of **Powersim** follows after a brief narrative of the flip-flop architectures chosen for study. A comparative analysis was performed on the chosen architectures using **Powersim**. The results so obtained are reported. The capabilities of **Powersim** are highlighted. To conclude, certain insights have been drawn to aid the designer in making an intelligent choice of the flip-flop architecture according to design specifications.*

Keywords: *Low-power, flip-flop architectures, Powersim*

1. Introduction

Digital designs are usually a composite mix of flip-flops interspersed with the combinational logic blocks. Due to their tremendous switching activity and a comparatively larger area, the flip-flops hold the maximum share in the entire power dissipation of the digital design. A suitable choice of architecture for the flip-flop therefore becomes a crucial aspect of digital design since this entails a remarkable impact on the total power budget of the chip. Apart from power, several other issues like area, delay and robustness can govern the choice of flip-flop architecture. But, if power is the prime requirement then one can possibly compromise on other aspects. The extent of trade-off is quite a design-level issue from which are extracted the specifications which rule upon the cell-level designer for his choice of the flip-flop architecture.

2. The Architectures and Design Guidelines

Hardware Realization of a Digitally Controllable Neuron Activation Function and its Derivative for Extremely Low Power Application

Amit K Gupta and Navakanta Bhat*

Abstract

A low-power CMOS circuit to generate both nonlinear sigmoid neuron activation functions and their derivative is presented. Neuron activation function is digitally controlled to switch between logsigmoid and tansigmoid. All the transistors of the circuit are working in subthreshold region in order to consume low power

1. Introduction

The model of each neuron in the multilayer feedforward neural network includes a nonlinear activation function that is monotonically increasing and bounded from above and below. The transfer characteristic of neuron, described by the input/output relationship $y_j = f_j(s_j)$ should be such that $\partial f_j/\partial s_j$ exists and is finite. Where y_j, f_j and s_j are output, neuron activation function (NAF) and input to the neuron respectively.

Significantly large number of components can be monothically integrated because of small silicon area and low power dissipation of analog elements whereas digital elements consume large silicon area and significant electrical power [6]. Neurons that can meet above requirements are given in [1-4]. Neurons in [1-2] have current inputs and voltage outputs and [3-4] have voltage inputs and current outputs. Transistors in [1-3] are operating in saturation, which results in large power dissipation and sigmoid-like activation functions. Neuron in [4] generates only logsigmoidal activation function. Unlike [1-3], the present circuit utilizes hardware to generate two neuron activation functions (NAF) which results in efficient hardware utilization. The circuit of [2] requires high degree of precision in order to switch between logsigmoidal and tansigmoidal.

A popular choice for neuron activation function is the sigmoid function defined by

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POWER AWARE CHARACTERIZATION OF SEQUENCE OF INPUT VECTORS FOR STANDARD CELL BASED DIGITAL CIRCUITS

P. K. Jain[1] **D. Boolchandani**[2] **V. Sahula**[2]

Abstract

Minimization of power consumed by digital circuits is important for a wide variety of applications, both because of increasing levels of integration and the desire for portability. Standard cell based design approach is preferred over full custom design to achieve the short design time. One of the ways to minimize power consumed by a digital circu it is to organize sequence of its input vectors so that during transitions of input vectors, switching activity at the nodes of the circuit is minimized. We show that the problem of search of minimum power sequence of input vectors is equivalent to search for minimum weight Hamiltonian circuit in a completely connected graph, and is NP -complete. Hence, this power minimization approach is feasible for small circuits only, like standard cell based circuits. This paper proposes a heuristic to find the sequence of input vectors for standard cell based circuits such that the power dissipation is minimum. We consider layouts of small digital circuits with n inputs where $2 \leq n \leq 4$. *We use TSPICE simulations to measure switching power and total average power consume d in a circuit under consideration.*

1 Introduction

An important attribute of a cell based circuit for most applications is to minimize the power consumption. The dynamic power contributes a major portion to the total power dissipation. The dynamic power di ssipation in static CMOS circuits depends primarily on the number of logic transitions per unit time. As a result, the average number of logic transitions per operation can serve as the basis for comparing the power dissipation of a variety of arithmetic c ircuit designs. In this paper, we propose a heuristic to characterize the sequence of input vectors' transitions so that the internal switching activity and hence power in the circuit is minimized. We present results of application of the heuristic on different cell-layouts and compare them with those provided by 0 -1 ILP, an exact algorithm.

2 Power estimation

An accurate estimation of power dissipation during various phases of VLSI design can verify the power dissipation requirements and thereby avoid

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Design of Broadband Controller for Residential Gateway Applications

Anindya Saha, Pankaj Saxena, Vikas Mishra, Rajesh Mundhada, Kamal Katiyar, Suresh Kumar, Arindam Saha[*]

Abstract

As Internet technology becomes more pervasive, homes are getting connected to Cable or DSL. The increasing user demands for "always on" service along with multiple connectivity for Voice and Data is gradually making presence of Residential Gateway in every household a reality. A Residential Gateway should have routing and bridging capabilities along with seamless connectivity to contemporary premise networking technologies. Integration of all these features on a single device essentially requires a rich architecture, smart design techniques and thorough verification.

This presentation describes the architecture and design of a Broadband Network Controller which is a critical component of TI's Voice and Data Centric Residential Gateway solution. The Residential Gateway consists of this broadband network controller and programmable Broadband transceivers (ADSL or Cable). It provides glueless interface to voice line interface circuits for "voice over" applications (like VoIP,VoATM,VoDSL) while at the same time provides support for premise networking technologies such as Ethernet and USB. Systems built with this controller are expandable in many ways by taking advantage of the integrated PCI interface which in turn could connect to devices such as USB Host Controllers, HPNA Transceivers etc. The chip consists of a MIPS32™4Kc™ processor as the host and dual-core C54x DSP subsystem together with peripherals interconnected via TI's proprietary on chip bus interface. The figure below shows the architecture of the controller which is further described in the presentation.

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Effective Utilization of Memory in Shared Memory Architecture

Pramod A. Chordia*

Abstract

This paper presents an effective memory utilization technique using *Memory Block-Linkage* Method in a shared memory architecture for switches and bridges. Memory is virtually divided into blocks and the blocks are dynamically assigned to different ports of the switch for storing the packets. Memory utilization should be as efficient as possible to reduce the requirements of the total system memory. Smaller the memory block size, the more efficient the memory utilization. Memory and hardware complexity requirement for maintaining the status of packet is proportional to the Memory blocks required for storing the packets. Memory Block-Linkage Method is presented in this paper for maintaining the status of each packet, which uses optimum memory. Also the scheme is introduced to keep statistics of the memory blocks i.e. allocation, de-allocation in the memory Block-Linkage method. Programmable size and the number of blocks, facilitates *design reuse* in various protocols. The proposed method has been implemented in the *IEEE 1394.1 Bridge Portal* for buffering of the asynchronous packets, in which main memory is software programmable for the asynchronous and isochronous traffic (IEEE 1394.1 Bridge Portal completed in Controlnet India Private Ltd.).

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FIR Filter for A law and μ law Data

Uma Mudengudi[+], Nalini Iyer* and Meena M[#]

Abstract

This project is a team work of 32 students and is carried out as part of Institute-Industry interaction with KARMIC Manipal, as a part of DUMPOYEE programme. The proposed project concentrates on maintaining nearly constant SNR with reduced computational complexity. Speech processing plays a major role in the field of telecommunication. It involves sampling and quantization of speech signals. Nonuniform quantization gives steps of variable size and is accomplished by companding. The most commonly used companding techniques are A-law and μ -LAW. The presence and the extent to which the noise degrades the performance of a communication system is measured by output signal to noise power ratio. The function of the receiver is to extract the input signal from the degraded version of the transmitted signal through the channel. The major blocks of a typical receiver are amplifiers and filters. In this proposed project the FIR filter implementation is achieved with reduced computational complexity by keeping fairly constant SNR and thus reducing the hardware requirements. The SNR has been maintained constant by neglecting the insignificant product after each multiplication. It can be extended to discard insignificant received data points. The project is simulated using MATLAB and C programs. The designs are implemented using free-ware tools SPICE and MAGIC on LINUX platform. Designs are carried out for 0.35μ technology.

Specifications:
Frequency 3.6MHz-100MHz.
Number of transistors: 11116.
Total area: 331852.52$(\mu m)^2$
Number of I/O Pads: 24.

1.Introduction

Successful communication depends on how accurately the receiver can determine the transmitted signal. Perfect signal identification might be possible in the absence of noise and other contaminations but noise is always present in electrical systems. The presence of noise superimposed on a signal limits the receiver's ability to correctly identify the intended signal and there by limits the rate of information. The extent to which the noise affects the performance of the communication system is measured by the output SNR.

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Finite Impulse Response Filter Design Using Chinese Remainder Theorem

Savitha*

Abstract

This project (**HI**gh speed **FI**lter **DE**sign using **C**hinese remainder theorem-**HIFIDEC**) is the combined effort of a small group of eleven undergraduate students of NMAM Institute of technology, Nitte. This is for the first time that such a work is being carried out in our college. The work is part of an effort in 'NET-KarMic Microelectronic Research Centre' set up when E and C, E and E and CS departments of NMAMIT, Nitte have joined hands with KarMic.

In this work, we present the implementation of Finite Impulse Response (FIR) filter using Chinese Remainder Theorem(CRT). To achieve high speed computation several carry less methods are possible. One such method is use of residue number system (also called Chinese Remainder Theorem). Each number is defined as a set of residues of relatively prime module set. A unique property of such residues is that multiplication, addition, subtraction and several other calculations can be carried out within each modulus. This residue set can therefore be used to uniquely represent the output of the filter which forms the key to our design consideration. Early use of such filters was in RADAR filtration applications and such number systems have also been used recently in cryptography.

The project required us to arrive at a reasonable modulii by simulation, design small width multipliers and appropriate modulo circuits. The modules were designed by hand routing standard cells provided by KarMic using MAGIC. The cells were simulated using SPICE. Verification of the design was also completed using freeware tools. This project was a challenge for us.

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DESIGN SYNTHESIS AND PHYSICAL DESIGN OF CMOS OPERATIONAL AMPLIFIER FROM USER SPECIFICATION

S. C. Bose[+], Abhijit Karmakar[+], Chandra Shekhar[+]
V Sunitha[*], Vigyan Jain[*], Gourav Jain[*],
Vishal Kulshreshta[*] and Robince Mathew[*]

1. Abstract

The growing need for integration of mixed analog-digital systems requires the automation of analog design process to expedite overall design. But, the design of analog circuit blocks still requires expert knowledge and hence even today, fully automatic analog circuit synthesis tools are not available. In this work attempt has been made to develop a point CAD tool that will convert the user specifications of Miller and RC compensated operational amplifier (op-amp) into a sized transistor topology. The user inputs include : Gain Bandwidth (unity gain frequency), Input Common Mode Range (CMR), Slew Rate (Sr). The aspect ratios (W/L) of all the transistors involved, the biasing voltages, dc gain, SPICE netlist and layout are the outputs of the CAD tool.

2. Introduction

The demand for cost reduction and improved performance resulted in the need for integration of both digital and analog circuits on the same chip. However, not only such integration but also pure analog circuit design require automation of the analog design process to expedite overall design [6]. Several approaches like (i) Optimization Based Design approach [5] (ii) Layout based design approach [7] (iii) Knowledge based approach [8] have been tried for design automation of analog circuits. Present work aims to evolve a complete design synthesis CAD tool based on a set of ordered equations for CMOS op-amps which are important circuit blocks for many analog sub system designs [1,3,4]. Thus, the automated design of an op-amp would greatly contribute to the [1]reduction of design cost and also design time of analog circuits. The input to the tool is the set of performance parameters of the op-amp and the output is the layout of the circuit.

This objective has been achieved in two steps: by developing two specialized CAD tools. The first tool generates the sizes of transistors for the topology of the op-amp starting from user specifications which include (i) unity gain frequency (ω_0) (ii) input common mode range (iii) slew rate(Sr). The aspect

+ CEERI, Pilani, * Students of CEERI-BITS ME (Microelectronics) program during the course of this work.

A Novel Approach To Unified RF Front End IC Design For Wireless Application

Prashant Admane, Biju Viswanathan,
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ABSTRACT

This paper describes the RF front-end chip-set for wireless application containing a high power SPDT switch, a Low Noise Amplifier and a Power Amplifier. A novel design approach has been adapted to carry out the designs to achieve the best possible performance on various parameters like low noise figure, high speed, low insertion loss, good linearity and good power added efficiency. A single process technology has been identified to realize these conflicting specifications on to a single environment. The philosophy of realization of all these designs as cascadable blocks has eased the integration issues as a single chip-set. The novelty of the design is that it is the sub-system realized on a single chip as well as the chips can be provided individually as an independent IC. As described in the paper, all the chips required for the chip-set have been designed independently in such a way that they can be interconnected easily, accordingly the input and output port directions have been determined. The tile, consisting of all these circuits is under fabrication, at present.

INTRODUCTION

The wireless communication is witnessing rapid growth in the number of subscribers, as it overcomes the limitations of wired-communication systems, providing advantages like mobility, greater productivity, cost saving, portability, high speed, reliable data communication, etc. Hence the wireless systems are being considered and used as replacement or extension to wired communication systems. The wireless communication systems utilize the electromagnetic waves to transmit and receive data using air as a channel. This brings out a golden opportunity for RF industries to prove their ability in commercial markets. Since the field is commercial, it is essential to pay attention on providing compact, low power and affordable RF IC solutions. This is the inspiration behind the design and development of a unified RF front end chip-set as per IEEE 802.11b standards for 2.4 – 2.5 GHz W-LAN applications.

The chip-set under discussions in this paper can offer a unique solution to various applications like W-LAN using IEEE 802.11b standard and latest IEEE 802.11g for the frequency band of 2.4 – 2.5 GHz as the RF front end is going to be unchanged. Similarly provisions have been provided to utilize the same chip-set for bluetooth applications also.

For wireless applications, the complete solution of RF front-end transceiver has been planned. This converts the received signal to IF level and IF signal to RF level for transmission. Accordingly the entire chip-set has been catered into two parts, Wherein high power SPDT switch, LNA and Power

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Comparative Study of RF Tuned Amplifier Performance with Different Inductor Configurations

R Srinivasan , C Venkatesh and Navakanta Bhat*

Abstract

In this paper, the performance of an RF tuned amplifier has been studied with three different realizations of inductors namely, spiral inductor, impedance emulated inductor and MEMS inductor. Quality factor and gain over a range of frequencies have been studied and the relative merits and demerits are discussed.

Introduction

Advances in CMOS technology have made it possible to integrate onto a single chip a communication system operating in the range between 0.9 and 2.5GHz, which can be used in mobile phones and global positioning systems. Almost all these communication systems use tuned amplifiers as their integral part. The performance of a tuned amplifier heavily relies on LC circuit employed in it. Of these, inductance is particularly difficult to realize in compact form together with a reasonably high 'Q'. The multi turn coil is a well-known direct technique to fabricate inductors in integrated chips. The other method to realize the inductor is by emulating the behavior of an inductor using resistance, capacitance and active devices. A much more recent technique is to use MEMS technology. A common source amplifier is frequently used as a tuned amplifier. The LC network connected between the V_{dd} and drain of the transistor is designed to produce a peak gain at the desired frequency. Section II discusses about the impedance emulator technique to mimic the behavior of an inductor. Section III discusses about the modeling of the spiral inductor with and without substrate effects. The MEMS inductor essentially corresponds to "no substrate effects" case wherein the substrate is removed by bulk micro machining. Next section deals with the tuned amplifier. Finally the simulated results have been presented and discussed.

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A NOVEL SINGLE HBT FRONT-END BASED MONOLITHIC OPTICAL RECEIVER

P. Chakrabarti and R. K. Lal*

ABSTRACT

The speed and reliability of long haul optical communication link can be greatly improved by making use of monolithic OEIC's (Optoelectronic Integrated Circuits). The optoelectronic integrated circuit involves integration of electronic and optical devices and/or components. From the technological point of view, the practical realization of OEIC's faces a number of challenges. Compositional and structural differences between photonic devices and electronic circuits are responsible for the problems associated with epitaxial crystal growth, planarization for lithography, electrical interconnection *etc* in monolithic integration. The technology of III-V semiconductors has matured significantly over the past decade. Monolithic integration of optical sources, detectors with other active components have been achieved using III- V materials. More complex system based on OEIC technology has also been realized in recent years. In this paper we introduce a novel concept of using a single heterojunction bipolar transistor (HBT) to play the dual role of a photodetector and pre-amplifier. The schematic circuit diagram of the front-end is shown in Fig.1a. The structural detail of the HBT is shown in Fig.1b. The design and analysis of the proposed single HBT front-end based optical receiver has been presented in this work. A rigorous noise model of the receiver has been developed to estimate its sensitivity as a function of operating bit rate. The performance of the proposed receiver has been compared and contrasted with the existing OEIC receivers (Fig.2). It is seen that the sensitivity of the proposed HBT based receiver is much better than the existing receivers including the newly proposed single MESFET based receiver. The proposed OEIC receiver supposed to be built using state-of-the-art InP/InGaAs technology. The proposed receiver has been found to exhibit a high transimpedence gain (~ 65 dBΩ), large bandwidth (~22GHz) and a very high sensitivity (-48.79 dBm at 20 Gb/s) in 1.55 μm wavelength region. The proposed OEIC receiver is expected to outperform the existing systems and emerge as a powerful alternative in future generation optical fiber communication. Use of a single HBT in the front-end would greatly simplify the fabrication of optoelectronic Integrated circuit receiver in the monolithic form.

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Poly-reoxidation Process Step for Suppressing Edge Direct Tunneling (EDT) Through Ultrathin Gate Oxides in NMOSFETs

Kingsuk Maitra and Navakanta Bhat[1]

Abstract

In this work, we identify polyreoxidation as a process step for selectively thickening the gate oxide at the edges (in the gate overlap region), and hence for suppressing the edge component of direct tunneling (EDT) through ultrathin gate oxides in NMOSFETs. It is shown that by varying the different polyreoxidation parameters viz: temperature and polyreoxidation time it is possible to achieve different levels of gate oxide edge thickening. This essentially implies that a desired level of gate leakage current may be maintained without modifying the gate oxidation process significantly.

Introduction

Direct Tunneling current from the gate overlap region into the S/D extension region (also identified in current literature as edge direct tunneling or EDT [1]) has been identified as the principal source of off-state power dissipation in state-of-the-art VLSI chips [2]. K.N Yang et. al. [1] has also shown that this component of gate leakage exceeds even BTBT (band-to-band tunneling) and GIDL (Gate induced drain Leakage) for ultra thin gate oxides in NMOSFETs. When the gate electrode is biased in the negative region, the gate overlap region over the SDE region immediately goes into accumulation given the fact that the flat band voltage between the heavily doped n+ region poly-Si region and the heavily doped region is almost zero. However, the poly gate region over the p-type substrate remains in depletion until $V_g=V_{fb}$. (for the poly gate and the p-type substrate), where the said flat band voltage is approximately is –1.0 V. These accumulated electrons in the gate overlap region tunnel into the depleted source drain extension region giving rise to edge direct tunneling. In this work, we try to develop a means by which EDT may be reduced. [2] has mentioned that this may be achieved by tuning the polyreoxidation parameters viz: polyreoxidation time and temperature by selectively increasing the oxide thickness in the overlap region. In this paper, for the first time we perform explicit process and device simulations to investigate whether the magnitude of EDT can indeed be decreased by following the said methodology. It is instructive to note here that a large overlap is a trend in modern VLSI device

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Self-Consistent Solution of 2D-Poisson and Schrodinger Wave equations for Nanometric MOSFET modeling for VLSI/ULSI purposes

S. Dasgupta and Deepesh Jain*

For the past 40 years, the electronic computers have grown more powerful as their basic sub-unit, the transistor has shrunk in dimension. Electron lithographic techniques are nearing their theoretical and economic limits for the production of more dense integrated circuits for VLSI/ULSI purposes. The solution to further need lies with the nano-meter scale MOS based as well as other devices that build upon experience with microelectronics but take advantage of the very same Quantum Mechanical Effects (QMEs) that limit the operation of microscale MOS devices. It is hoped that nano-meter-scale replacements can continue the miniaturization of the computational and information storage elements to the molecular level with expectations for vast increases in memory density, power and performance. The present paper provides a numerical approach to solve consistently two-dimensional Poisson's equation and Schrodinger wave equation under a set of boundary conditions. The quantum as well as classical charge has been computed. The quantum charge is a direct function of Density of States (DOS) and the classical charge can be found out by simply solving the two-dimensional Poisson equation under specific boundary conditions. The channel voltage profile and electric field profile has also been presented. The results obtained indicate that the classical model underestimates the channel voltage and the longitudinal electric field in the channel as compared to that obtained through Quantum Mechanical (QM) approach. The study assumes importance in the light of the fact that the devices in near future would assume nanometric scale and hence this approach to modeling will give much more realistic output characteristics of nano-MOS based devices.

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STATISTICAL MODELING OF 0.1μm NMOS DEVICE CHARACTERISTICSFOR IMPLANT DOSE VARIATIONS

H. C. Srinivasaiah and Navakanta Bhat[1]

Abstract

Statistical analysis is performed for the four important implant dose parameters namely halo, SSRC, deep s/d and s/d extension implants characterizing the NMOS devices in 0.1μm technology node. The factorial design of experiment is used to perform the analysis. Second order polynomial regression model is developed for some of the important device characteristics such as saturation region V_t, (V_{tsat}), drive current in saturation region ($I_{dsatdrive}$), leakage current in saturation region ($I_{dsatleak}$), subthreshold slope in saturation region (SSsat) etc. Various model diagnostics like residual analysis and coefficient of determination, are performed to study the accuracy of the model for each of the device parameter.

Key words

0.1μm CMOS Technology, Halo, SSRC (Super Steep Retrograde Channel), RSM (Response Surface Methodology), Regression Technique, residuals, DOE (Design Of Experiment).

1. Introduction

The device structure in the DSM regime is becoming more complex in order to suppress the short channel effects, (Taur *et.al*, 1997). One way of improving the device speed significantly without excess short channel effect is to use special implantation steps like, halo, SSRC (super steep retrograde channel), deep s/d (source/drain) and s/d extension implants, (Taur *et.al*, 1997 and Xu *et.al*, 2001).

As the scaling has entered DSM regime the number of process variables to be controlled to minimize the mismatch between devices due to inherent process variations has increased enormously . The variations in implant dose parameters, is a major concern which affects the device/circuit performance, (Srinivasaiah and Bhat , 2002) .

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LAYOUT DESIGN OF CASCODE CURRENT MIRROR WITH IMPROVED CURRENT MISMATCH

D. Dhawan[1] **D. Boolchandani**[2] **V. Sahula**[2]

Abstract

The performance of analog Metal-Oxide-Semiconductor (MOS) integrated circuits depends heavily upon the element of matching accuracy. Matching accuracy of current mirror is especially important in analog IC performance. Layout techniques and device size are believed to be the major factors that can improve the matching behavior to a large extent. Though this information is important, there have been limited studies or research done on these two factors. In this paper, we propose a new layout technique for cascode current mirror based on proposal of Lan et al [1999] for simple current mirror. The new layout for Cascode current mirror improves the matching characteristics in the presence of parameter gradient. Effects of threshold gradient across a transistors' active area on the matching characteristics of current mirrors are discussed. New and the existing layouts of cascode current mirror are compared using SPICE simulations for threshold voltage gradients at all angles across the active area. Results show a significant improvement in matching characteristics of the proposed structures for cascode current mirror over what is achievable with existing layout techniques.

1 Introduction

As the field of VLSI (Very Large-Scale Integrated Circuit) design advances, the demand for higher precision analog circuit design also grows inevitably. The realization of any precision analog circuit design has to begin with a thorough understanding of the matching behavior of the devices because the performance of the analog circuits depends heavily on the matching of the devices.

Presently, the most popular technology for realizing microcircuits makes use of Metal-Oxide-Semiconductor Field Effect (MOSFET) transistors, and it is expected to remain the dominant IC technology for the foreseeable future. Thus, the study of the matching behavior of MOS transistors remains important because the performance of analog MOS integrated circuits depends heavily upon the element of matching accuracy; refer Lakshmikumar et al (1986). Device layout technique and device size are two important factors that affect the matching behavior of any design of MOS analog circuits. The layout of integrated circuits is the central problem in high-density chip design. There is one mismatch component present in MOS devices which is not present in bipolar transistors, and that is the mismatch of the threshold voltage. Thres hold

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A Search Scheme To Solve the Complex-Triangle Elimination (CTE) Problem For Unweighted Adjacency Graphs

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Abstract

This paper presents a valley-descending search scheme to solve the complex-triangle elimination (CTE) problem for unweighted adjacency graphs with arbitrary level of containment. Elimination of all complex triangles (CTs) is an essential step of VLSI floor-planning through rectangular dualization approach. Recently this has been proved to be NP-complete [8]. The basic scheme presented in this paper has been made more efficient by introducing knowledge at the initialization of search. Performance of the scheme has been compared with a heuristic, as well as a simulated annealing (SA) based algorithm. Experimental results show that the informed valley-descending (IVD) scheme is the best. SA produces solutions of same quality. But its convergence is slower than that of IVD. This indicates that perhaps the state space of this problem do not contain any local optima. However, this is yet to be proved (or disproved).

Keywords : *Rectangular dualization, Valley-descending, Floor-planning, Level of containment, Simulated Annealing (SA)*

1. INTRODUCTION

Rectangular dualization [1-7] is an important approach to VLSI floor-planning. The input to this phase is an adjacency graph G_{ad}, whose nodes represent functional blocks and the edges represent interconnection between the blocks corresponding to its end vertices. In unweighted adjacency graphs no weight is attached to the edges. In rectangular dualization approach each module is realized as a rectangular area in the floor-plan. Here G_{ad} is triangulated, i.e., each face of G_{ad} is made a triangle. When converted to a floor-plan the nodes of G_{ad} map to rectangular areas and the edges map to shared sides between these rectangular areas (*Fig.1.1*). Before we formulate the problem addressed in this paper, a few terms that are used throughout the paper, are defined below.

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LaySeq: A New Representation for Non-Slicing Floorplans

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Abstract

In this paper, we propose LaySeq a new representation for non-slicing floorplans and show its superior properties. Layseq uses only n[lg n] bits for a floorplan of n rectangular blocks. The solution space size of layseq is just O(n!). This is very smaller than that of all recent representations. Given a layseq it takes only linear time to construct the floorplan. Layseq is very simple and easy to implement representation. Based on this new structure a hybrid genetic algorithm for floorplanning is given. We show that layseq is efficient in handling rectilinear blocks too. Experimental results show that layseq results in smaller silicon area than earlier approaches.

1. Introduction

Due to increase in design complexity, circuit sizes are getting larger. IP blocks are intensively used to reduce the design complexity. This trend makes floorplanning or building block placement much more critical process. A fundamental problem in floorplanning lies in the representation on geometric relation between the modules. The representation directly affects the quality of the floorplan/placement and the complexity of the process. Thus it is important to develop an efficient representation for floorplan/placement design.

1.1 Previous Work

VLSI floorplans are often grouped into two categories, the *slicing structure* [5] and the *non-slicing structure* [1, 2, 3, 4, 6, 7]. A binary tree whose leaves denote modules can represent a slicing structure, and internal nodes specify horizontal or vertical cut lines. Wong and Liu proposed an algorithm for slicing floorplan designs [5]. They presented a normalized Polish expression to represent a slicing structure, enabling the speed-up of its search procedure. However, this representation cannot handle non-slicing floorplans. There are $O(n!\ 2^{3n-3}/n^{1.5})$ combinations of the slicing tree structure. It takes only O(n) time to derive a floorplan from a representation. Recently, researchers have proposed several representations for non-slicing floorplans, such as sequence pair [6],

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eSpec : Specification Solution Driving Cell Create Flow

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Abstract

Designing to specifications is a key care -about for cell designers. However the current ASIC cell design methodology does not have a defined process for specification capture. Subjective interpretations of cell functionality, redundant and inconsistent data views for different work-flows and lack of robust check mechanisms affect the quality of libraries at the expense of designers' valuable time. This paper describes eSpec as the new specification methodology driving the cell design flow that addresses these issues. eSpec segregates specifications into technology dependent and independent vectors. It prescribes capturing functional specification in Verilog and the library, cell characteristics in the newly devised eSpec format. This extensible format allows hierarchical specification across library, cell groups and cells and allows overriding across these levels. It enables easy mechanisms of setting up the characterization inputs, its migration across technologies and correct by construction methods for deriving stimulus for characterization and modeling. eSpec drives mechanisms for creation of early access libraries with predictive characterization data and generation of CAD models. eSpec also functions as a reference for various checkpoints that ensure higher quality of cell deliverables. With eSpec based flow, designers will be able to spend more time on actual cell design to deliver better libraries.

1. Introduction

In the nanometer era, decreasing size and increasing size due to integrating multiple components on a single chip require the last drops of performance to be squeezed out of CMOS technology. The growing uncertainty of performance together with the need for more complex functionality makes extra analysis and more painstaking design a must -do for the ASIC cell designer.

ASIC libraries have to be rapidly defined, developed and delivered faster and when the technology node is made available. Different flavours of libraries are required each tuned for performance, area and power to cater to a wide variety of market segments. The library portfolio needs to be rich, with a variety of differentiated, high-speed cells, which shall be of high design complexity. Libraries also need to always remain in tune with the Spice models from the silicon fab to provide full silicon entitlement. Influencing the library design further is the chip create methodology and tools . To meet these critical careabouts, we need a robust Cell create system which cuts down on the library generation time without compromising on accuracy and integrity of the deliverables.

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An analytical approach to determine cross-talk noise in VLSI chips

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Abstract

In deep sub-micron technologies, the coupling noise, which is also known as cross-talk noise can cause functional failures. Conventional cross-talk analysis produces pessimistic results and gives too many aggressors and victims. This paper presents an analytical approach to arrive at a reduced set of aggressors and victims, which are more likely to affect the functionality of the design. In this approach, we estimate maximum noise coupled to a victim net for time period long enough to cause functionality failures. We also discuss the effect of rise and fall time of aggressors on victim net. This analytical approach drops spurious aggressors and victims and results in saving significant amount of simulation time.

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AN ACCELERATOR FOR FPGA PLACEMENT

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Abstract

In this paper, we propose a constructive heuristic for initial placement of a given netlist of CLBs on a FPGA, in order to accelerate the iterative phase of the placement in the context of re-configurable computing. The experimental results of our method show significant improvement in cost compared to the initial placement of the popular tool VPR. We observe that simulated annealing converges much faster given the proposed initial placement configuration.

Keywords: *FPGA, Placement*

1. Introduction

Placement in an FPGA is the process by which a *netlist* of circuit *blocks* (which are either *I/O* or *Configurable Logic Blocks (CLBs)*) is mapped onto physical locations which is essentially a two dimensional array. Placement algorithms are broadly classified as constructive methods and iterative improvement techniques. Constructive methods build up a solution step by step starting with a single unit. Iterative improvement algorithms start with a valid initial placement and repeatedly modify the configuration with the objective of reducing a certain cost such as delay, wire-length, area, etc. Iterative algorithms produce good placements but require enormous computation time which may depend on the initial configuration of the placement. Typically, many trials are performed with various initial solutions. The iterative phase may however be *accelerated* by starting with a good initial configuration.

In the context of reconfigurable co-processors, it is essential to reduce the time complexity of mapping, place-and-route stages without sacrificing the quality of solution. From earlier works, we find that most of the FPGA placement algorithms are iterative. With this motivation, we propose in this paper a fast constructive placement algorithm for a given *technology-mapped netlist* of *CLBs* on an island-style FPGA, realizing a given digital circuit.

2. Earlier Works on FPGA Placement

FPGA placement techniques can be categorized as force directed methods, Tabu search, successive bi-partitioning or quad-partitioning and clustering based algorithms. There are many works on bi-partitioning and quad-partitioning techniques for placement [Takahashi (1995), Krupnova (1997)]. Work related to clustering based techniques is extensive in the literature [Lou (1998), Senouci (1998), Fang (1997), Tsay (1995)].

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High Performance Routing for VLSI Circuit Synthesis

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Abstract

In VLSI layout design it is required to realize a specified interconnection among different modules using minimum possible area. This is known as the routing problem. There exist several routing strategies for efficient interconnection among different modules. One of the most important types of routing strategies is *channel routing* [4, 8]. A channel is a rectangular region that has two open ends and the other two sides have two rows of fixed terminals. A set of terminals that need to be electrically connected together is called a *net*. The terminals of the same net are assigned the same number. The unconnected terminals are assigned the number zero.

Throughout the paper we consider the *reserved layer Manhattan routing model*, where only horizontal and vertical wire segments are used for interconnecting the nets [4]. The layer that has only horizontal (vertical) wire segments is called a *horizontal (vertical) layer* H (V). The connection between a horizontal and a vertical wire segment of the same net in two such adjacent layers is achieved using a *via hole*.

The *channel routing problem (CRP)* is the problem of computing a feasible route for the nets so that the number of tracks required (and hence the channel area) is minimized. We assume that the routing wires do not extend beyond the left and right ends of the channel. Therefore, in order to minimize the routing area, the horizontal wire segments of the nets need to be distributed amongst a minimum number of tracks. This process of assignment of the horizontal wire segments to tracks is guided by two important constraints viz., the *horizontal constraints* and the *vertical constraints*. These two constraints are represented by two important constraint graphs viz., the *horizontal constraint graph (HCG)* and the *vertical constraint graph (VCG)*, respectively [4, 8]. An undirected edge $\{v_i, v_j\}$ in the HCG indicates that the corresponding intervals I_i and I_j are *horizontally constrained* and are not assignable to the same track in the channel.

The *local density* of a column is the maximum number of nets passing through the column. The *channel density* is the maximum of all the local densities. We denote channel density by d_{max}. Each of these d_{max} nets must be put in distinct tracks of the same horizontal layer.

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SPEED AND AREA OPIMISATION IN SRAM BASED FPGAs

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1. Introduction

Field Programmable Gate Array (FPGA) technology permits the design of many complex digital circuits using a single off-the-shelf device. Although FPGAs provide a low-risk, low-turn around time option for implementing digital circuits, they suffer from slow speed and low density circuit implementations as compared to conventional circuit implementation techniques. Much of this area and speed penalty is due to the programmable routing structures contained in the FPGA. By optimizing these routing structures, significant performance and density improvements are possible.

In this paper we focus on the optimization of Configurable Logic Block (CLB) and Routing Architecture. It is shown that a cluster based CLB with four 4-input LUTs, a fully connected Interconnect Matrix, segments of only length 4 and Masud's Switch block is the optimal architecture to achieve best results with respect to area and speed.

This paper is organized as follows: Section 2 contains a brief introduction to the FPGA architecture and the terminology used in this paper. Section 3 contains the general experimental method followed. Section 4 deals with the design of CLB architecture and Section 5 discusses the Routing architecture. Section 6 presents conclusions and precisely states the contributions of this work.

2. Architecture Overview

Logic is implemented in FPGAs using many Basic Logic Elements (BLEs). These BLEs are grouped into Logic Clusters or Logic Blocks. Within a logic block, the BLEs are connected using a programmable routing structure called an Interconnect Matrix, as shown in Figure 1. The Interconnect Matrix is a programmable switch matrix that connects:

- BLE outputs to BLE inputs within the same logic block
- Logic Block inputs to BLE inputs.

These programmable switches are usually implemented using a pass transistor controlled by the output of a static RAM cell. By turning on the appropriate programmable switches, right connections can be made between the logic block inputs and outputs.

Figure 1 shows Island-Style FPGA architecture. In island-style architecture the Logic Blocks are organized in an array separated by horizontal and vertical programmable routing channel. A Switch Block is used to make connections between the tracks in adjacent channels. Figure 1 shows only one switch block and one logic block, but real FPGAs consist of many switch blocks and logic blocks. The Interconnect Matrix within a logic block and the fixed tracks and programmable switches outside of the logic blocks are collectively known as

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Single Event Upset Response of a 0.09μm SRAM cell using 2D and 3D simulation

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Abstract

In this paper we have carried out 2D and 3D simulations of Single Event Upset (SEU) phenomenon on a 0.09μm technology SRAM cell. Although we obtained the identical Linear Energy Transfer (LET) value to flip the 2D and 3D cell, the details of the charge collection mechanism are quite different for these two cases. This work compares the relative merits and demerits between the Full-3D and Full-2D simulations.

1. Introduction:

In the space radiation or nuclear environment, the high energy particles such as electron, protons, alpha particles, and cosmic rays pose a certain radiation risk to all electronics component. If such particles strike the sensitive area of CMOS ICs such as SRAM memories, it could results in Single Event Upset by flipping the memory data.

Device level simulations are very time consuming simulations since they solve coupled Poisson's and continuity equations in the entire device. In order to reduce the computational time, Mixed-mode method is one of the commonly used technique to characterize the SEU (Single Event Upset). There are several ways of performing the Mixed-Mode simulations. One of the methods is defining the sensitive NMOS at device level (either 2D or 3D structure), and others are at SPICE level. The later will reduce the simulation time as compared with full 3D simulation, but simulation would not be able to capture the cross coupling between the transistors. Slight modification to this method is defining all the four transistors at device level which we have considered for our work as one of the two simulation techniques described here. But still it is not good enough to capture the above mentioned effect. The full-3D simulations is capable of capturing the phenomenon like latch-up which is impossible to see in the other simulation methods without proper modeling [1]. Despite being so accurate it is a very time and resource consuming technique as for our simulations it takes around 2.5 hours for 2D and 4.5 hours for 3D up to the feedback time. Comparing 3D and 2D results tells the effect of neighboring junctions on the radiation generated charge. We have chosen 0.09μm SRAM technology for our simulation work which has significant effect of it's own neighboring junctions on the radiation parameters due to shorter geometry

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REPEATER DESIGN CONSIDERATIONS FOR VLSI INTERCONNECTIONS

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Abstract

The propagation delay, power dissipation and chip area are a few of the major design constraints of a very large scale integration (VLSI) circuit. It is envisaged that the VLSI technology level would reach its limits of 0.05 micrometer by the year 2012. With minimum feature size of the devices on integrated circuits reducing to such low levels, the component size has been highly scaled down and component density increased manifold, as a consequence the length of the interconnections in a VLSI circuit has enhanced by orders. These long interconnections lead to a large propagation delay of the data and clock signals. The insertion of optimal number of CMOS repeaters or buffers at apposite points in these interconnections not only reduce such delays but also decrease power dissipation Lin.

The various design considerations of the long interconnections in VLSI are presented in this paper. A comparative study of uniform repeaters, tapered and cascaded tapered buffers is given here. The results are verified using OrCAD SPICE. In the present study the interconnection is modeled as a resistive capacitive (RC) and resistive inductive capacitive (RLC) load.

Keywords
Interconnections, VLSI, Propagation delay, Repeaters, Buffers.

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Clock Tree - Wish List v/s Facts

Kamran Nabi Khan*

Clock Tree Synthesis is one of the most critical parts of the Physical Design Flow. As the requirements and design constraints go tighter and tighter, the need is felt for more and more accurate, advanced, intelligent and flexible clock tree synthesis tool. The clock tree is expected to perform better in the most complex clock structures available today. The skew values, the phase delays, the inter-clock balancing, the transition times, maximum capacitance etc., have very tight requirements and yet the results are expected to be achieved with minimum number of CTS buffers to minimize congestion and save area and power.

Enormous amount of work has been in this area, and many of the people working in this area have come up with a variety of clock configurations, clock balancing, and other techniques to achieve better performance. This paper mainly concentrates on Clock Tree Synthesis from the user's point of view. Presented in this paper is the wish list of clock tree synthesis vis-a-vis the study of tools available today. Here a relative study is done on various clock tree synthesis tools available today. This includes distinguishing features of Avanti's GCTS and Astro CTS, Cadence's CTGen and CTPKS, Silicon Perspective's CTS tool, Synopsys' CTC and Ultima's ClockWise.

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ON EVALUATION OF PARAMETRIC YIELD FOR AN OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

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Abstract

Any manufacturing process has natural variations, even when it remains within its control limits. Inevitable fluctuations in the manufacturing processes and environmental operating conditions of the integrated circuits cause circuit parameters to vary randomly about their nominal target value. The concept of parametric yield loss of ICs arises because of the des ign intolerance to these variations. Such losses are due to the effects such as mask mis - alignments and implant dose variations over a whole lot of wafer and dice. It can be distinguished from catastrophic yield loss, which is loss due to local effects such as dust particles. The global effect in turn induces variations in process parameters such as sheet resistance of the MOSFET oxide, Capacitance C_{ox} and threshold voltage V_T that lead to different instances of the IC having different performance, see O'Leary (1995).

Many methods have been used to predict parametric yield of Analog Ics, see Becker and Jensen (1977), Elias (1994) and Yu et al (1987). Some of these methods are Normal approximation, convolution method, direct mapping and Monte-Carlo simulation. The Normal approximation technique is based on expansion of a function around a feasible solution point (in our case the desired parameters of the unit under consideration) to yield multidimensional Taylor series which can be approximated to a linear ex pression with the assumption that the input values are Independent and Identically Distributed (IID) with Gaussian Probability Distribution function. The Gaussian PDF used is actually a Gaussian curve truncated at $\pm 3\sigma$ points. The Chebyshev inequality for these points is .003. Hence to normalize the truncated PDF we divide each of the values by 0.997. The convolution method is based on the assumption that change in output variable is the sum of the changes caused by varying the input variables individually. The method of direct mapping is a multidimensional convolution scheme to take care of two or more output variables simultaneously.

Monte Carlo method is based on computer simulation, simulating the process, which takes place on a production run such as t o pick up at random a component for the case of defined maximum parameter variations. This method allows any number of output variables to be considered irrespective of the fact that they are linear or nonlinear functions of inputs. We have chosen this method, as it is amenable to computer simulation. The only drawback is that to

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Two-dimensional Numerical Modeling of Sub-0.25 μm MOSFET for VLSI Applications

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Abstract

MOSFET is a basic component of VLSI (Very Large Scale Integration) and ULSI (Ultra Large-Scale Integration) circuits. Large packing density, low noise and low power consumption make MOS devices an attractive choice for application in electronic systems. Even more remarkable is the pace with which the downscaling of transistor has taken place from about 10 μm to the deep sub-μm range permitting over 10000 times more transistors to be integrated on a chip. The numerical model presented here solves two-dimensional Poisson equation in the depletion region of MOSFET under certain boundary conditions, which are governed by the physics of the device. The solution of the Poisson equation and extensive mobility modelling helps in evaluating the surface potential and electric field of a deep sub-micron MOSFET.

MEMS for Space Applications: An Overview

S.V Sharma, M.M Nayak*, Arun Batra, N.S Dinesh+

Abstract

Several types of sensors, actuators and fluidics are used in the integration of the state of the art Satellites and the Launch Vehicle for proper operation and health monitoring of the various sub-systems and the System as whole. Some of the sensors used in the Space program are Pressure, Level, Temperature, Force, Acoustics, Accelerometers, Gyroscopes, and Optical Sensors like Earth Sensor, Sun Sensor and Star Sensor etc. Few types of actuators and mechanisms used are Relays, Pyro cutters, Solar array deployment mechanisms, Antenna deployment Mechanisms, Thrusters, Valves, Solar array and Antenna drive mechanisms etc. The major requirement in the Space program is the requirement of the device to perform reliably during various ground testing and also under the harsh Space environment. The key word in Space technology is the reliability. In addition to the worst Space environment like wide variation in temperature, Vacuum, and radiation (electron, proton & heavy ions) the device will face worst ground environment like humidity, dust, and also severe mechanical shock & vibration during launching. In this paper an overview of development of Micro Electro Mechanical Systems (MEMS) technology for the Space application, its requirements and advantages are discussed.

1.0 INTRODUCTION:

Space systems comprise more than just Spacecraft; they include launch vehicles and the ground-based systems used for tracking, command, control, and data dissemination (pictures of the Earth, telephone calls, Tele Vision via Satellite, etc.,). Electronics pervade almost all Spacecraft systems. Individual electronic components can be classified as purely electronic or electromechanical. Purely electronic components (e.g. inductors, resistors, transistors, ICs etc.) do not require any physical movement for proper operation, while Electro-Mechanical components (e.g. quartz crystal oscillators, relays, surface acoustic wave (SAW) filters, variable capacitors, and potentiometers) require translation, rotation or vibration. Co-fabrication of both purely electronic and electromechanical components on the same substrate is possible using a combination of MEMS and semiconductor fabrication techniques. This approach leads to a reduced part count, volume, and the number of microscopic electrical interconnects. Miniaturization of mechanical systems promises unique opportunities for new directions in the progress of science and technology. Micro mechanical devices and systems are inherently smaller, lighter, faster, and usually more precise than their macroscopic counterparts and consumes very less power.

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Trends In MEMS Fabrication Technology

K.Natarajan*

INTRODUCTION

Micro Electro Mechanical Systems (MEMS) refers to devices that have a characteristic length of less than 1mm, but more than 1 micron and combine electrical and mechanical components that are fabricated using semiconductor-processing technology. Conventional manufacturing techniques for MEMS included Bulk Micro-machining and Surface Micro-machining. After more than 20 years of development, MEMS devices are revolutionizing in the 21st century requirements from automotive systems to Microbiology. Commercial production of MEMS devices is growing at the rate of 30% and the projected market potential is about **US$ 30 Billion by 2004**. Considering the growth, a large numbers of companies in the world are entering into MEMS based devices and systems.

MEMS devices have a unique advantage of reduced size and weight for a given function and realize electrical, mechanical, chemical, optical and thermal functions incorporated on a single chip. Highly innovative techniques are being adopted for the manufacture of these devices. Diverse technologies and innumerable applications have resulted in non-standard specifications and package technologies, which prevail presently for these devices. Currently, the MEMS devices required for the Indian market are imported and the market size is **Rs.200 crores**. The major areas of use are Defense, Aerospace, Space, Industrial and Commercial. For the last 2 years, increased awareness of this technology, both in the research level and industrial level have enabled increased interest for use of the devices. The emerging MEMS market is focusing on bringing together silicon based microelectronics with sensor and actuator technology, making possible the realisation of complete **systems on a chip**. MEMS technology makes possible the integration of microelectronics with active perception and control functions, greatly expanding the design and application space and having a dramatic impact on everything from aerospace technology to bio-technology. Silicon remains the prime substrate for these devices.

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DESIGN, MODELING AND SIMULATION OF POROUS SILICON MEMS PRESSURE SENSOR FOR SPACE APPLICATIONS

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Abstract

This paper presents an approach for designing a porous silicon MEMS pressure sensor, which uses porous silicon (PS) as the distributed RC network layer. The pressure applied changes the piezoresistance R resulting a change in impedance. This property is utilized to form a phase detecting electronics, where we get a signal phase change with applied pressure. The sensor has been designed for a pressure range of 30 bar typically for space application. Design consideration, modeling and simulation of the sensor are presented.

Keywords: *Pressure sensor, MEMS, diaphragm, porous silicon, RC network, phase detection.*

1.Introduction

Porous Silicon (PS), formed by electrochemical anodization of single-crystal Si substrate in an appropriate electrolyte solution, has found a variety of applications in microelectronics, optoelectronic devices [1], and micro electromechanical systems (MEMS). PS finds its use in MEMS devices such as accelerometer, pressure sensor [2], atomic force microscopy (AFM) probes; and semi-permeable gas membranes [3] and capacitive sensor for chemical vapor sensing [4]. PS can be looked upon as an effective medium of three phase mixtures of silicon nanowires, SiO_2 and voids. It is equivalent to a distributed RC network of which R is piezoresistive. The membrane of the porous silicon MEMS structure when subjected to a pressure undergoes variation in its piezoresistance like normal piezoresitive silicon, but unlike them develops a phase shift as well across its terminals like a capacitive sensor. The developed phase shift is proportional to the impressed pressure and may be processed and detected suitably by an integrated signal processing phase detector circuit. Other than this, there are other advantages of PS MEMS over the conventional MEMS. Besides having a very large surface to volume ratio, widely variable pore sizes

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Property Specification and Extraction within an Assertion-Based Verification Framework

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Abstract

Assertion-based verification—that is, user specified properties and automatic property extraction combined with simulation and formal techniques—is likely to be the next revolution in hardware design verification. This paper explores a verification break-through prompted by multi-level specification and assertion verification techniques. The emerging Accellera formal property language, as well as the Open Verification Library standards and the important roles they will play in future assertion-based verification flows are discussed. Furthermore, automatic property extraction techniques are explored—and the important role they play when validating semantic consistency in the context of an RTL signoff flow.

1 Introduction

Silicon transistor capacity, the ability to utilize these transistors in a design, and the time required to verify the resulting designs are all considerations that drive the system architect's decisions about planning the next generation system-on-a-chip. While silicon capacity continues to increase along the Moore's Law curve (enabling the designer to create very large systems), the effort required to verify these larger designs has increased at an even greater (and thus alarming) rate. Essentially, silicon capacity is doubling every 6 months. Furthermore, the designer's ability to utilize this larger silicon capacity has increased approximately ten-fold within the past decade due to the widespread acceptance of synthesis technology. However, the ability to verify larger systems has not kept pace. Rather, verification productivity has experienced only incremental improvements during the same period. Thus, what is clearly needed in verification techniques and technology is a revolution in design verification—the equivalent of the synthesis productivity break-though that allowed a ten-fold increase in design productivity.

In order to address increased verification complexity, methodologies must be improved through more effective techniques, which include a combination of traditional simulation, formal constraint driven block-level smart simulation stimulus generation, semi-formal bug-hunting techniques, and formal property checking. Assertion-based verification, or property specification, is the key ingredient for improving verification methodologies. This paper discusses the important role of property specification and automatic property extraction in the context of an assertion-based verification flow.

1.1 Property specification

One organization that works to support improvements in verification methodologies is Accellera (see www.accellera.org). Their mission is to drive worldwide standards that enhance a language-based design automation process. Recently, the Accellera Formal Verification Committee proposed standardization for the formal property language *Sugar* [Accellera 2002]. This *declarative* property language supports *top-down* (that is, functional specification-driven) design methodologies. Declarative property languages are ideal for specifying architectural and global properties, as well as defining interface specification during block-level partitioning.

In addition to adopting Sugar, the Accellera Assertion Committee has developed a standard for specifying RTL implementation properties directly within the designer's HDL through the *Open Verification Library* (OVL) [Foster and Coelho 2001] and the new *SystemVerilog* procedural assertion construct [Foster et al. 2002]. The OVL provides a template for expressing a broad class of assertions *structurally* within the designer's RTL, while the new assertion construct facilitates expression of assertions *procedurally* during RTL development. Both the OVL and the new assertion construct enable *bottom-up* (that is, white-box) verifiable implementation practices, which improve simulation-based methodologies while providing a seamless path to formal verification.

Combined, these powerful and expressive formal property languages enable engineers to:

System Level Verification of Present Day System on a Chip (SOC)

Vishal Dalal[1]

The complexity of present day SOC's is increasing tremendously with more and more components (IP's) put on a single piece of silicon. As designs become complex there verification becomes more and more complex. It may be relatively straight forward to design a unit level module, but, to correctly integrate it in an SOC is challenging. In other words to verify a design in a complete system's perspective is really demanding. Although the components are rigorously verified individually, the main focus at system level verification is on checking the integration between the various components. This task become further difficult as many IP's are from different vendors and may not have desired or correct interfaces. Therefore, at system level we need to verify the interfaces between various components. We also need to verify different Hardware and Software scenarios that may occur in a system. In this paper we explore the verification of an SOC at system level. We discuss the problems at system level verification, its complexities, the Hardware-Software co-verification methodology and its usefulness.

One of the significant requirements of a good verification is a correct metric to indicate the progress and effectiveness of verification. In order to have an effective metric to indicate the usefulness of test cases or verification, we need to define the *functional coverage* i.e features of design covered by test cases. The functional coverage will not only indicate test base effectiveness but will also help in writing new test cases to hit the uncovered design features. In this paper we describe the functional coverage at system level, how we can define the coverage monitors to cover those functionalites and there usefulness.

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Applying Model Checking for Verification of Small Controllers

Satish Panigatti, Ambar Gadkari and Rubin A. Parekhji*

Abstract

Hardware verification has now been recognised as one of the most important phases in the VLSI design process. This is because of the absence of a proven set of criteria to establish when verification is complete, and the time required, in turn, to complete such verification. Formal techniques for hardware verification have been developed, and are projected to alleviate both the above problems.

In this presentation, the application of model checking techniques to industrial designs, in the DSP Design Centre, Texas Instruments (India), Bangalore, will be discussed. The presentation will cover (a) basic principles of model checking, (b) construction of properties to be verified for a given design, (c) specific situations where model checking can be effectively used, and (d) extensions to check for specific fail conditions. Three examples, namely the JTAG interface TAP (Test Access Port) controller, a Flash memory controller and a memory BIST (Built-in Self-test) controller, will be used to illustrate the above.

In the first example, important reachability properties were verified. In the second, the handshake mechanism inside the controller was verified. In the third example, the effectiveness (non-effectiveness) of the BIST controller for detecting modelled (non-modelled) faults was verified.

It may be emphasised that the designs considered are reasonably small to understand the operation of model checking and to compare it with traditional simulation based approaches. (The authors are also aware that model checking has been used to verify much larger designs).

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Using Formal Techniques for Identifying Uninitialized Registers in SOC Designs

Anindya Saha and Rajendra Ranmale*

Abstract

SOC designs today comprise of IP blocks from different design teams and vendors. Because of differing design styles being used on IP's, integrating them and verifying them is a challenge for design teams. One of the problems encountered during design integration is that of implementing *system reset* or *initialization* circuitry. Incomplete knowledge of the IPs often causes problems late in the design flow, when we perform gate-level simulations with back annotated delays, thus uncovering a bug due either to incorrect integration or incorrectly assumed behavior. Uninitialized registers in a design can propagate unknown values throughout the design and can pose problems in gate-level simulations. Identifying uninitialized registers in a design can be a time consuming process given the complexity of the designs today. This paper describes how formal verification techniques are used in identifying uninitialized registers in SoC designs. We model the transition relation of the registers using Binary Decision Diagram (BDD). We assert the reset condition by constraining the design ports to constant logic values. Under asserted reset conditions, the BDDs can be reduced to constant values. The reduced BDDs represent the initialized value of the registers. Registers that cannot be reduced to constant values under asserted reset condition remain uninitialized. Hence a register can be identified as uninitialized if the BDD has more than one terminal vertex. We discuss the scenarios in which the registers in a design can get initialized, and propose a methodology to identify the uninitialized registers. This BDD based approach is faster compared to conventional approaches and can be easily implemented with formal verification tools.

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EXTERNAL MEMORY INTERFACE: A METHOD FOR FUNCTIONAL VALIDATION OF DIGITAL IP ON TESTCHIP

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Abstract

This paper presents a method of functional validation of digital IP's embedded with 8-bit microcontroller at test chip stage, having feature of **External Memory Interface**. At test chip stage, usually emulators are preferable and simple to test functionality versus user specification in real environment. Assembling and delivering the emulators for the dedicated microcontroller takes two to three weeks. The proposed method has the advantage to speedup the validation process and generate the report without emulators, dedicated EPBs etc. Also this method bypasses the defects or bugs due to the Internal Memory or the System program, and validates other digital IP's successfully.

Microcontroller, under test, has been configured for external memory interface by the software and necessary hardware connections has been made with an external EPROM, on an application board. A general purpose **Memory Emulator** has been used for programming the test software. Test software can be developed in "assembly" or "C" language and **Error conditions** have been inserted for each check points for **automatic check**, which has been displayed on **LCDs**, connected on the application board. This method has been successfully applied for validating digital IP's like 16-bit Timers, Serial Peripheral Interface, and On Screen Display for ST9 families of microcontrollers designed by ST Microelectronics.

1. Introduction

Today, Time to market and the Quality are the two important governing factors for success of the product. Customer must receive well-tested and qualified product. Mostly after fabrication of a VLSI chip, there is a design validation activity to test that chip on silicon, which is done on the TESTER, here the objective is mainly to test the fabrication/process related issues and functionality

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DESIGN FOR RANDOM PATTERN TESTABILITY OF ASYNCHRONOUS CIRCUITS

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Abstract

The testability of CMOS VLSI circuits correlates with the switching power that they dissipate. Improvement of testability features of a CMOS circuit leads to an increase in its switching power dissipation. So, design for testability and design for low power dissipation are in direct conflict. This conflict can be resolved by separating the testing issues from low power issues so that the circuit can operate in normal operation mode and test mode. The parallel random pattern testing technique described in this paper uses the probabilistic properties of the 2 -input XOR gate. The state registers and the combinational circuits are tested in parallel. The proposed bit parallel random test technique provides for the bit serial scanning of test patterns into the state registers of the sequential circuit. This makes the testing faster than the traditional scan test. The har dware redundancy of the proposed approach depends greatly on the complexity of the combinational logic block. The testable sequential circuit designs have been implemented using four-phase circuits. The test complexity of sequential circuits designed using the DFT techniques is reduced to the complexity of testing just their combinational parts. An asynchronous implementation of the BILBO technique has been demonstrated on a micro pipeline design with BIST features.

1. Power Consumption of CMOS Circuits

The rapid development of CMOS technology makes transistors smaller allowing a chip to incorporate ever lager numbers of them (Weste 93). CMOS VLSI circuits are increasingly used in portable environments where power and heat dissipation are vital issues. As a result, the power dissipation of CMOS VLSI circuits is a growing concern for design engineers.

The majority of power estimation tools are oriented towards calculating only the average switching power of CMOS circuits using the following formula (Deng 94).

$$PW_{sw} = f * V_{dd}^2 \Sigma(P_{tri} * C_i)$$

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AN INTRODUCTION TO P1500

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Abstract

Increased usage of reusable cores in present day SOCs requires a core-based test strategy, in which cores can be tested as separate entities. IEEE P1500 Standard for Embedded Core Test (SECT) is an evolving standard that aims at improving ease of reuse of test and test vectors, especially if they contain cores from different core providers. This paper briefly describes the need for IEEE P1500 and the components of the IEEE P1500.

Keywords: *CTL, Firmcore, Hardcore, P1500, SECT, SOC, Softcore, Source/Sink, TAM, Unwrapped, Wrapped, Wrapper*

1. Introduction

A core based System-On-Chip (SOC) device contains multiple cores supplied either from within an organization or from a core provider or both. Design complexity and Time-to-Market concerns have lead to a Core-Based SOC design approach. Cores are pre-designed, pre-verified complex functional blocks. Core based SOC may also contain multiple instances of embedded memory, along with user-defined "glue" logic. Cores can be "soft" (i.e. mergeable and changeable), "firm" (i.e. mapped to gates but still changeable), and "hard" (mapped to silicon, non-mergeable). The cores used in an SOC may have the different attributes like different test technologies (muxed DFF, LSSD, LBIST, etc.,), multiple design abstraction levels (Soft (RTL), Hard (Gate level netlist), Firm (GDSII), different core providers and different vector formats (TDL, WGL, STIL etc.,).

2. Challenges in Core based SOC testing

Because of the different attributes of the cores used in an SOC, the testing of core based SOC is complex. Followings are the different challenges in testing core based SOC.

1. Cores are not manufactured and tested individually.
2. Ability to integrate a number of different reusable cores possibly supplied by different vendors, along with different test strategies.
3. If the core is HARD, DFT must exist before delivery - how to access and test complex cores when they are embedded in an SOC?
4. If the core is delivered with pre-generated vectors, how are vectors merged in the test program?
5. Test reuse and SOC level vector generation is complex and time consuming.
6. If the core operates at a different frequency from the other chip logic - how does this affect DFT and Test?

Test Access Architecture Design for SOC

K. Sudarsana Reddy and Santanu Chattopadhyay*

Abstract

System level integration is evolving as a new paradigm in system design, allowing entire system to be built on a single chip, using predesigned functional blocks called cores. Major problem in realizing core based systems is the adoption of adequate test and diagnosis strategies. The following are the most important issues in SOC testing:

- Testing cores with different functionalities coming from different vendors.
- Accessing cores from primary system inputs and primary outputs.
- Controlling the whole SOC testing process.

Since embedded cores are not directly accessible via chip inputs and outputs, special access mechanisms are required to test them at the system level. A number of test access architectures are proposed in literature which include *macro test*[2], *core transparency*[4], *dedicated test bus*[5], *multiplexed access*[6], and *TEST RAIL*[3]. Among these, TEST RAIL provides flexible and scalable test access mechanism. A single test rail provide access to one or more cores, and an IC may contain one or more test rails of varying width.

In [1], *Chakrabarty* has presented formal methodology for designing optimal test architectures for testing SOCs. He developed the Integer Linear Programming (ILP) models to find the optimal test rail distribution and the associated access mechanisms. Although ILP formulation gives the optimum results, they are not suitable for the systems with larger number of cores. In [1], results have been presented for ICs having maximum of ten cores. On the otherhand, many of the recently proposed *ITC benchmarks*[7] (to be presented in the International Test Conference (ITC-02)) have even more than 30 cores. For these systems, ILP will require enormous time to come up with the optimum solution. In this work, we propose a Genetic Algorithm based approach to solve the problems posed in [1]. Here we are presenting genetic algorithm formulation for the problem P1 noted in [1].

Genetic Algorithm Formulation:

Problem P1: Given N_C cores and N_b test buses of widths W_1, W_2, …… W_{Nb}, respectively, determine an assignment of cores to test buses such that total testing time is minimized.

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UNIFIED BIST AND FUNCTIONAL OPTIMISATION IN BEHAVIOURAL SYNTHESIS

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Abstract

Built In Self Test (BIST) has emerged as a promising solution for increasingly fast and dense VLSI circuits. Traditionally, the testability insertion phase comes after functional logic synthesis and verification in the VLSI design cycle. This creates two separate optimisation processes: functional optimisation and BIST insertion and optimisation. The first deals with functional design behaviour, while the second deals with test behaviour. In behavioural synthesis, considering testability at such a late stage in the design flow limits the efficient design space exploration as it contradicts the design methodology convergence requirements. It can lead to problems such as exceeding chip area, inability to achieve the required throughput, degraded performance, and inability to apply certain test methods efficiently. Unlike earlier work on "BISTing" data paths, we propose a novel method for inserting and optimising BIST structures at an early stage of High Level Synthesis.

Key Words *:* Built In Self Test (BIST), Control and Data Flow Graph (CDFG), High Level Synthesis (HLS), Behavioural Synthesis

1 Introduction

Improvements in VLSI technology gate density and increased clock speeds have made testing an integral part of chip design. With VLSI technology advances test equipment is failing to keep pace with this growing speed of circuits. Consequently, BIST has emerged as a promising solution to the test problem. Additionally, recent trends in systems-on-a-chip (SOC) design hampers the testability of embedded cores due to limited accessibility. This makes BIST the most suitable method for testing embedded cores in a SOC environment. In existing VLSI design flows; test structures are inserted after the functional design is complete. This can lead to unacceptable performance degradation, forcing a redesign of the system or re-synthesis for test (Parulkar (1998)). High Level Synthesis (HLS) allows architectural exploration such that user-defined functional design parameters like area, delay, and power can be traded against each other for an optimised RTL design. In this paper, we propose using a

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BOUNDARY SCAN IMPLEMENTATION AT SOC LEVEL

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Abstract
This paper deals with the issues and drawbacks of using IEEE 1149.1 JTAG complaint cores in a core based SoC.
Today's SoCs are largely designed using reusable cores. Testing of these embedded cores is becoming increasingly difficult. There are few ad-hoc techniques followed in the industry to test the cores of a SoC. Boundary scan IEEE 1149.1 standard may be used to test these embedded cores. The drawbacks and issues of using boundary scan for SoC testing is discussed in this paper.

1.0 Introduction

The core based SoC may consist of cores that already have boundary scan implemented. These cores will be reused in the SoC. IEEE 1149.1 [1] defines the implementation of boundary scan for top level of a chip, but doesn't define the requirements for core of an SoC. Hence the implementation and control of boundary scan inserted cores from the top level of a SoC is not defined. This will lead to more verification problems, as the implementation is not standardized. There is no definite verification methodology available as the integration of different TAP controllers at the top level is not pre defined and every designer will control them according to his application. This will lead to manual verification of the SoC, which is very complex and time consuming.

2.0 Testing using Boundary scan implementation at SoC level

Typically in a SoC, the boundary scan inserted cores will have individual tap controllers. In addition to this, the chip itself can have boundary scan inserted. In that case, the SoC follows a hierarchy i.e. there are many boundary scan implementations inside the boundary scan implemented chip fig1.

This situation cannot be captured and represented in BSDL. It would be a violation of boundary scan standard, due to the existence of multiple tap controllers in the chip.

The other possibility is that there could be one tap controller at the SoC level and no tap controllers at core level. This master TAP controller can control all the cores and testing of the cores can be carried out in a manner similar to board level test. If this method is to be adopted, an efficient addressing scheme to select cores is required. If memory bist is present in that core, then generating and routing the memory bist signals add to extra complexity.

Test Power Considerations in Testing of Core-based SOC

C.P. Ravikumar and H.T. Srinivas[1]

In multimillion gate designs, power dissipation during the testing of the chip is a big concern, since the test power can be several orders of magnitude higher when compared to functional power. In this paper, we address the problem of minimizing the peak test power dissipation during scan testing. We propose techniques such as test reordering and test insertion to address the test power problem. We show that the optimum test-reordering problem is equivalent to the Asymmetric Minimum-cost Hamiltonian Path problem and describe two solutions to this problem. The first is a greedy heuristic algorithm and the second is based on Genetic Algorithm. We show experimental results on ISCAS-89 sequential benchmarks. Up to 14% improvement in peak test power was noticed on the benchmark circuits.

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REUSE OF SINGLE STUCK-AT FAULT TEST SET FOR TRANSITION DELAY FAULT COVERAGE

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Abstract

In this paper a case study is presented, in which, test set generated for single stuck-at-faults in full scan circuit is used for testing transition delay faults and show the coverage. The transition delay fault coverage is found to be good with this test set. The advantages of using single stuck-at-fault test patterns for transition delay fault test are

1) If the transition delay faults coverage achieved is sufficient, then there is no need of generating extra vectors, or we can use this vector set and generate vectors for remaining fault coverage, this will save a lot of time.
2) Saving in tester time - The vectors applied at speed will cover stuck-at as well as transition delay faults at the same time. Only extra-generated vectors (if any, to cover remaining transition delay faults) need to be applied afterwards, thus saving tester time and in turn cost of testing.

Introduction:

The extremely tight timing constraints imposed on complex VLSI chips push the technology to the limit and drastically reduce the slacks along the paths. As a result, chips have become vulnerable to the delay faults. Such paths may be caused by either a parametric variation in the processing or a local defect, affecting either a transistor or an interconnect. It has become very important to test the transition delay faults.

Correlation between stuck-at-fault and transition delay fault test set:

Most of the work in the domain of delay fault has been based upon the slow-to-rise/slow-to-fall fault model. These delay defects are basically an adaptation of the stuck-at model to accommodate the delay faults within the classical test generation and fault simulation algorithms. However, this very often implies that either a single fault is injected or that the various faults are uncorrelated. When more than a single fault is allowed, faults can mask each other and this must be accounted for by generating robust tests, i.e., tests whose effectiveness is independent of delay defects at other locations. The approach to generate delay

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EFFECTIVE MEMORY TEST SOLUTION FOR ON-CHIP CACHE MEMORIES

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Quality and reliability of embedded memories is a critical aspect of the whole chip quality. For instance, in many designs today, logic may consume 60% of the silicon while memories may consume 40%. Appropriate techniques, therefore need to be employed for testing memories in a complex design for manufacturing defects, that not only test the memories efficiently and thoroughly but also meet the cost-of-test and time-to-market goals of the IC manufacturing process. BIST is a recommended optimal technique for SoC memory test when the design comprises of small number of large memories. But for memories that are small or are positioned on performance critical paths in the design (register files, cache, FIFO etc.), the area/timing overhead introduced by the BIST circuitry may not be acceptable. It would also be undesirable to alter the functional path of such memories in the design. Vector Translation is a non-intrusive test technique that enables the test of small and performance critical memories without inclusion of additional logic. Neither does it have an impact on the timing performance of the design. It automates the testing of embedded memories by automatically translating the functional patterns (sequence of writes and reads) for the memories into scan patterns. The scan patterns thus created for the embedded memories like cache could be merged with the scan patterns for the general logic on chip. Memory BIST and Vector Translation together help address memory test challenges for a memory intensive design.

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Introduction to AC_EXTEST

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Abstract

The use of AC-coupled differential signaling in high-speed designs is increasing by the day. High-speed circuit interconnect test is not possible with the existing IEEE 1149.1 EXTEST Sequences. For example, while testing high speed inter-connection defects that affect only one leg of a differential pair may be undetectable. This is because of the fact that Boundary-scan test is carried out at a lower frequency, hence the test may pass but this will lead to functional failures when the device is operated at high frequency. As Boundary scan has become an important criterion in all complex IC's for circuit interconnect testing, the same can be extended to test capacitor coupled nets. The testing of AC coupling has become a major criterion for designs containing boundary scan. Hence the need for testing these nets is increasing by the day. A method needs to be devised that can be integrated with the existing Boundary scan circuitry.

1 Introduction

AC_EXTEST is a proposed extension to the existing IEEE 1149.1 standard for testing capacitor-coupled nets. AC_EXTEST transmits information on transitions, whereas EXTEST transmits information on levels. The implementation of AC_EXTEST within the existing IEEE 1149.1 standard requires an overhead of bscan cells that support the AC_EXTEST instruction. This inturn will also require the generation of ac signals to capture and generate these transitions. The AC_EXTEST instruction is a superset of the existing EXTEST instruction. AC_EXTEST instruction when updated will target the Boundary register between TDI & TDO. Any component implementing the AC_EXTEST instruction should also support the EXTEST instruction. The bscan cells that support the AC_EXTEST instruction are capable of capturing & generating the transitions in a Run Test / Idle state of the TAP controller. In order to generate transitions required to transfer information during AC_EXTEST AC patterns are to be generated, The AC patterns applied by the AC boundary scan cells are a continuous stream of alternating "0" & "1". The capture and observation of the AC patterns is carried out in the Run Test / Idle state. This is carried out in the Run Test / Idle state as boundary scan allows the user to perform other tests while it stays idle in this state.

A control cell may be added to enable or disable the generation of AC patterns. When the AC cells are in the AC_EXTEST disabled state they should operate as the EXTEST instruction.

2 Components of AC_EXTEST

The implementation of AC_EXTEST requires the implementation of AC compatible bscan cells. We also need a mechanism that will generate control

A Comparison of Techniques for At-speed Testing

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Abstract

The classical stuck-at fault model is proving to be increasingly inadequate for screening out the defective VLSI chips after fabrication. Another fault model being increasingly considered is the delay fault model. Unlike the stuck-at fault model, it models the incorrect logical behaviour of a wire or gate with respect to time. This behaviour is because of defects which prevent the circuit from working at its operating frequency.

Testing for delay defects requires the chip to be tested at its operating speed, (unlike for stuck-at defects). This form of testing is termed as at-speed testing. In this presentation, various techniques for at-speed testing are reviewed and their effectiveness compared. These techniques include (a) application of functional tests, (b) at-speed application of normal scan ATPG patterns, (c) application of dedicated transition fault and path delay fault tests, generated using ATPG, and (d) application of at-speed tests using logic BIST.

The pattern generation and application process is explained for each of these techniques. Situations where the pattern sets are related are identified. The design support required for pattern application is also explained. A combination of these techniques has to be used to obtain a better set of at-speed test patterns, in terms of the defect coverage and test time. Experimental results, based on the application of these techniques to a DSP core design, will also be presented.
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Directed Search Based Optimal Test Vector Generation using Threshold Value Simulation

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Abstract

In the last few decades, advances in integration technology of circuits have made electronic circuits and systems more amenable for applications where high speed, high precision and high reliability are required. In the design cycle of any VLSI circuit, testing is one of the most important steps. Testing includes generating test vectors as well as testing the physical devices using an ATE. In this paper, we used the ideas of non-binary simulation techniques to help reduce the cost of test vector generation (TVG) efforts. In this paper new test vectors are found by optimizing a suitably defined cost function, using Threshold Value Models for non-binary simulations and Directed Search methods.

1. Introduction

As the complexity of the IC increases, the testing problem becomes more difficult and testing cost rise to as high as 40% of the total product cost [Shar85]. Therefore there is a need to evolve efficient algorithms for test vector generation, which will reduce time for generating test vectors and also give a minimal set of vectors that are to be used for testing the devices.

Defects like opens and shorts are the manifestation of most of the physical failures in VLSI circuits. Test vectors are required for detecting these defects. To analyze the faulty behavior and develop techniques to detect failures, abstract fault models that can represent most of the possible failures are required (single stuck-at-fault models are still widely used to comprehend most of the manufacturing faults).

The factors that are considered in selecting a test generation algorithm are

1. Number of vectors that are tried to generate the final set of test vectors
2. Number of vectors in the final test set
3. Fault Coverage

The work presented here covers the development of a test vector generation scheme for combinational circuits using the techniques of threshold value simulation and directed search. The primary objective of this work is to find and analyze different ways of reducing the test generation costs. The role of cost function in TVG is outlined in Section 2. The technique of Threshold

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FORMAL VERIFICATION OF FINITE STATE MACHINES

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Abstract

The classical methods of design verification of a digital design had been simulation and testing. Due to constraint of time, simulation based testing approaches use only a small sub set of input patterns whereas formal verification allows all input combinations to be taken into consideration. Model checking is one of the approaches of formal verification. The design description, modeled using the model verifier script, allows specification of some properties of the design using temporal logic. A synchronous sequential design can always be described as a finite state machine (FSM). The formal verification of an FSM is based on analysis of set of reachable states of the corresponding finite state automata. For large systems, state space explosion is main problem to deal with. Instead of describing large FSMs as flat description, we propose to describe FSM after abstracting non-essential group of states of the given FSM. This abstraction is a manual process and is guided by CTL formulae to be checked. We have used symbolic model verifier, public domain software, available from Cadence Berkeley Labs USA. We evaluate our proposal for some example circuist along with an 8-bit microprocessor.

1. Introduction

The classical methods of design verification of a digital design had been simulation and testing. Simulation based testing requires application of exhaustive input patterns to ensure functional correctness of the design. With the increasing demand for short time to market and larger complexity of the circuits, only sub set of input patterns is applied which is selected such that it ascertains a known level of fault coverage. This may lead to some errors in design remaining undetected and possible functional failure of the chip later. Formal verification allows all input combinations to be taken into consideration. Theorem proving and model checking are approaches popularly followed during formal verification. Theorem proving is less amenable to automation, whereas model checking allows high degree of automation for its algorithms.

In Section 2, we discuss briefly about various verification approaches for combinational and sequential circuits. A synchronous sequential circuit can always be described as a finite state machine (FSM). Section 3, contains discussion as how to describe and verify finite state machines. We propose to describe large FSMs as hierarchical description to a model checker, instead of a

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Formal Verification for Validating Processor Architectures

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1 Introduction

Functional verification of a design is a critical step in the overall IC fabrication process. There are three main methodologies to functionally verify designs: Simulation, Emulation and Formal verification. Test generation and semi formal methods can also be seen in this broader classification. Each of these methods is popular within the industrial environment. With the rise in chip complexity and shrinking time to market constraint formal methods are looked upon with renewed interests. They also have the ability to detect bugs at an early stage and also to uncover some of the hardest and corner cases at a much faster speed. We consider a formal hardware verification problem to consist of formally establishing that an implementation satisfies a specification. Though formal verification techniques have been applied to various hardware designs and memory arrays this paper focuses on designs related to processor architecture.

There are three main approaches to formal hardware verification: Theorem proving, Model checking and Symbolic simulation. Each of these methods or a combination of them is used to validate a design by checking proof of logical correctness, equivalence of models (Equivalence check) or some properties of models (property check). While the first approach still needs manual interference the other two are quite mechanized and automatic. A distinctive feature of theorem proving is that it is structural rather than behavioral in contrast to the approach of model checking. The main disadvantage of model checking is that it suffers from state space problem. Though newer techniques like use of BDDs and symbolic model checking are employed to overcome this problem still it is limited to small problems in practice. Thus model checkers are best suited to validate temporal properties of finite state systems like control paths in a processor. Theorem proving is best suited for data dominated verification where the state space can be large or unbounded. One of the major advantages of symbolic trajectory simulation is that it is possible to use sophisticated circuit models without having to know the details of the models. STE is also a restricted methodology as compared to theorem proving but is more efficient than theorem proving. Since proof checking and model checking are complimentary technologies, many of these tools are used in unison. The HOL/VOSS system is an early attempt in this direction. PVS and propositional mu-calculus model checker is yet another example to combine proof checkers with model checking. Attempts have also been made to integrate temporal logic model checkers like SMV and language containment systems such as COSPAN with PVS. Several companies like Intel etc. have also integrated proof checkers, model checkers and STE tools within their in house developed formal

Design Methodology for Multi-million Gate Hierarchical Designs

Suresh Honnenahalli[1]

Chip design and chip integration are becoming more and more complex as we move from 0.18 micron to 0.13 micron to 90-nanometer technology. Understanding the issues involved in designing such high complexity chips is extremely important, in order to minimize the design cycle time and minimize Cost Of Deployment of the product.

The following topics will be covered in the workshop:

- Deciding on the right methodology
- Point-tools based flow vs. fully integrated design flow
- Sign-off quality tools
- Pre-qualification of Libraries
- Challenges of Timing Closure
- Challenges of Clock Trees Synthesis
- Avoidance, analysis and correction of Signal Integrity problems, such as, cross-talk, electro-migration, and IR drop
- Power planning and implementation
- Problems related to DFT implementation
- Manufacturability issues
- Flip-chip design

In hierarchical designs, timing closure is number one concern in the back-end, and timing issues dominate the RTL-to-Tapeout time. In VDSM technologies, silicon integrity issues, such as, cross-talk, electromigration, and IR drop, add to the usual problems of timing closure. In addition, the foundry's manufacturability rules for antenna, metal-slot, and via-reliability are becoming more and more complex with each process generation. The place and route tools and analysis tools need to support these new rules.

The timing problems are introduced at the very beginning of the flow, where wire load models are used during synthesis. For one, this makes the flow very iterative, and at the end of the day, does not guarantee timing-closure. Also, in point-tools based flow, there is mismatch in timing between Synthesis, P&R, and external sign-off Static Timing Analysis tool. There is a mismatch of RC values between Place & Route tool and external sign-off RC Extractor. Some of the other factors that affect timing closure are slew degradation over long wires, long wire buffering, placement optimization, signal integrity, and simultaneous Clock Tree Synthesis of multiple domains.

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Perspectives on VLSI Industry and Education in India

M.J. Zarabi[1]

Abstract

In this new economic era, world economy is going to be driven by information and knowledge based industries rather than traditional industries in which microelectronics/very large scale integrated circuits (VLSIs) is expected to play a key role. In this emerging hi-tech economy battle, advancement of the nations will be closely related to their ability to innovate and build new VLSI products which inturn will depend upon the number of skilled engineers in this area that they are able to produce and deploy.

In India the culture of building integrated circuits completely from design to manufacturing was initiated by Semiconductor Complex Limited (SCL) in the 1980s. However, this activity has not quite proliferated yet and has also not kept pace with advancements abroad. Even while a number of design centers by well known Semiconductor Companies such as TI, Motorola, ST Microelectronics, Analog Devices, Cypress, etc. have been set-up to cater to their in-house design needs, independent Indian Design Houses set-up in the late nineties are primarily providing design services. If India is to play a significant role in this hi-tech area in the world market it would require to play strength in terms of intellectual properties and innovative products. Any effort in that direction would require to be strongly backed-up with sound policy and infrastructure for quality education and training of large number of our engineers in this area.

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Integration Issues in Implementation of Student LSI Design Projects

Shivaling S Mahant-Shetti*

Abstract

Silicon has defined our current civilization much as bronze and steel defined earlier ages. A unique ability of silicon is to dramatically reduce cost of products, a companion quality to mass utilization. With India's vast numbers, silicon use in Indian products therefore holds vast promise, possibly more than what it has done for western markets. Many of India's care abouts are different from those in the west (and east) and hence solutions are different. Disposable income in the west is a higher quantum than in India and more complex products built with expensive technology form the majority of products. To cater to Indian market, lower cost products produced by less expensive, more mature technology is useful. We believe therefore that there is a need for transistor level design engineers even if it was not coming back in fashion. Having understood circuit design at such level, they would be able to appreciate underlying issues in ASIC VLSI much better.

The work of Mead and Conway would not have been as powerful if there was not MAGIC, SPICE and MOSIS to go with it. Ability to commit an idea to a layout, fabricate the design and then debug produced excellent chip designers. Designing small circuits that are affordable to fabricate and provide this training is extremely valuable. We are on the verge of being able to do this in India now.

Step by step learning is necessary to understand IC design. These are:

1. Metal Programmable Gate Array
2. Standard Cell IC design
3. Memory Design
4. Analog/Power IC Design

With the familiarity of TTL style digital design, a metal programmable gate array provides an early entry in the Indian context. Processes available in Indian Fabs have only a couple of metals and almost half the cost and time is saved using this approach. An additional advantage is ability to protect a novice engineer from easy mistakes such as I/O I, ESD issues and power supply distribution issues. After some familiarity, a standard cell based digital design would help a more compact design where issues of speed area tradeoff and pitch matching etc can be tried. Third level of complexity comes in analogish memory design followed by full analog design. The cost of software has hindered VLSI education in India greatly. The tools used in our efforts are essentially free and hardware is low cost (estimated at about Rs 3 lakhs to train 24 engineers).

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Software Engineering Practices in Student Projects

Suresh Kumar*

Abstract

Computer Science/Engineering had been the only "privileged" discipline to have software development even in late 90's in bachelors' and masters' programs in India. However, use of computers and development of software, are part of almost all engineering disciplines today, and the domain of VLSI is no exception. For example, in the area of VLSI, a large number of student projects are related to VLSI design activity using EDA tools and development of new EDA tools. Several of these projects are closely linked to sponsored research projects undertaken by the faculty of the academic institutions, as part of their active interest in industry interaction and industry-sponsored research. The success of these programs relies, to a large extent, on the success of the student projects, and its results to get deployed in the industry. Software development as an engineering discipline is many times overlooked while executing such projects and lack of this discipline sometimes become the main reason for the failure of the projects. Student projects can benefit immensely by adopting software engineering practices. This talk will highlight the importance of software engineering practices in student projects, and its relevance to a future career in industry.

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Project Management in VLSI Organizations

S. Ramesh*

In the *ASIC Product Development* division of TI, the ASIC Design Kit product delivery is a development effort involving over 200 engineers spread across 12 teams from India, USA and Japan. In this global development environment, the role of inter-personal and inter-group communications, inter-group coordination, and tracking is vital to the success of the project. Since projects have tight timelines, it is important that all stakeholders clearly understand the goals, objectives, scope, and plan of the project. Changes in customer requirements during project execution impact schedule and/or scope, reactions to these changes from the stakeholders must be timely and in alignment with the goals of the project. In this presentation, I'll share the experience of the ASIC Product Development team (APD) in managing *TimePilot* and *Pyramid* programs.

The presentation is organized into four sections. The first section describes the project planning and tracking process. I'll discuss how the development team arrives at an initial plan despite incomplete input information. I'll describe how we manage task partitioning and inter-team handoff. I'll also focus on how we deal with changes in input information that is external to APD, and how we attempt to absorb the changes without impacting the customer commitments. The second section of the presentation deals with the communications infrastructure used within the organization across development teams to remain in sync with the project expectations and deliverables. I'll describe the periodic and asynchronous review procedures used to achieve this synchronization. In the third section, I'll focus on how an individual teams assess the system-wide impact of a change that the team incorporates in its individual piece. In the last section I'll address the attainment process, which includes weekly teleconference among project leaders from teams world-wide in order to maintain the project focus and ensure project success.

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The New Recruits in an IT Company: A Behavioral Perspective

Anand Kasturi*

The Information Technology industry in India has witnessed immense growth in the past five years. There are a large number of multinational companies and their subsidiaries that operate from India. A job in a vibrant and dynamic area such as Information Technology can be both rewarding and challenging. Other than training the newly recruited engineers in technical skills, companies today devote a significant portion of their resources in training them on behavioral aspects such as team-working skills, inter-personal communication, and professional ethics. This talk will focus on the behavioral aspects of a budding Indian engineer, with insights into the source of the positives and negatives in the behavioral pattern of the engineer.

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VLSI Technology and Design: Frequenty Not Asked Questions

Nagaraj Subramanyam*

The areas of VLSI technology and design are constantly changing and evolving. It is difficult for an engineering curriculum to keep pace with this dynamics. In the VLSI Education Day held at Bangalore in 2001 as part of the VLSI Design & Test Workshops (VDAT 2001), we organized a session on "Frequently Not Asked Questions," where a panel of experts from industry faced technical questions from the audience in an open forum. This session was an immense success. Questions varied from the very basic to the very advanced. What is an antenna check? What is meant by Built-in Self Test and why is it necessary? Are there portions of the data path that really operate in 1 ns time-frame? What is the speed of the fastest gate built to-date? This year, we wish to hold the FNAQ session once again at VDAT 2002 for the benefit of students, faculty, and other participants of the workshops.

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Continuing Evolution of High Tech Economy: How Can India Arrive at the Scene

Nitin Deo[1]

Over the past few decades we have seen changing economic picture and how different countries have arrived at the scene. First it was the U.S. with innovation and invention, then it was Japan with manufacturing prowess, now Taiwan and China have arrived at the scene with cheaper, higher quality alternatives. In the coming few years, India has a real chance to arrive and stay at the world economic scene.

There was a time when software and hardware were two different links in a chain. They are merging very rapidly and that's where India has the opportunity to excel once again - just as it excelled in the software market.

In a review of various trends in the systems market - mainly communications and consumer fields - it becomes clear that customized solutions with custom-designed ASICs and software running on it, provide the necessary differentiation. But this requires a good understanding of the hardware platforms including design of complex systems and chips along with application software.

India has secured its place in software world, with highly talented research, development and support engineers. Now is the time for Indian high tech community to get involved in research, development and support aspects of semiconductor and system design. The best way to start is to partner with key systems and semiconductor companies from U.S. and Europe. And within just a few years, India too can arrive at the scene and stay.

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An Interdisciplinary Computer Engineering Curriculum

Vishwani D. Agrawal[1]

For evolutionary reasons computer engineering is often regarded as a branch of electrical engineering. Computer science, on the other hand, maintains a distance from electrical engineering. Considering that both computer engineering and computer science have sufficiently matured, they deserve a separate but unified identity. This talk presents a Computer Engineering curriculum that combines basic sciences, mathematics, and engineering courses. The graduates of this program should be able to work in any environment where computers are either built or used. The need for such a degree program is fundamental in today's society, which refuses to do anything without computers. Besides the fundamental or core skills, the curriculum would contain electives for specialization into various other engineering domains, such as architecture, civil, communication, chemical, electrical and mechanical, as well as non-engineering fields like entertainment, media and law. It is this last part that makes the computer engineering curriculum interdisciplinary.

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