Digital Circuit Testing and Design-for-Test

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Presenters

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Outline - Day 1

- Introduction (9:00 am – 10:00 am)
- CAD Tools (10:00 am – 10:30 am)

Coffee Break

- CAD Tools (contd.) (11:00 am – 11:30 am)
- Logic Test – Basics (11:30 am – 12:30 pm)

Lunch

- Logic Test (2:00 pm – 3:00 pm)
- Advanced Fault Models (3:00 pm – 3:30 pm)

Coffee Break

- Advanced Fault Models (4:00 pm – 5:00 pm)

Outline - Day 2

- Power Aware Test (9:00 am – 10:00 am)
- DFT (10:00 am – 10:30 am)

Coffee Break

- DFT (11:00 am – 11:30 am)
- Logic BIST (11:30 am – 12:30 pm)

Lunch

- Logic BIST (2:00 pm – 3:00 pm)
- Memory Test (3:00 pm – 3:30 pm)

Coffee Break

- Memory Test (4:00 pm – 5:00 pm)

Outline - Day 3

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- Test Compression (9:00 am – 10:30 am)

Coffee Break

- Test Compression (contd.) (11:00 am – 12:30 pm)

Lunch

- Fault Diagnosis (2:00 pm – 3:30 pm)

Coffee Break

- Fault Diagnosis (contd.) (4:00 pm – 5:00 pm)

Outline - Day 4

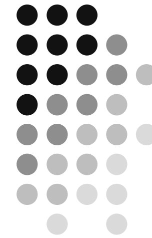
6

- Industrial Practices and Experiences

Advances in Test/DFT

C.P. Ravikumar

Noida, Aug 17, 2007



Agenda

- Process Variation
- Variability Issues in Test
- Power-aware Test Generation
- From DFT to DFTMY

Acknowledgements are due to the authors of various papers cited in the foils