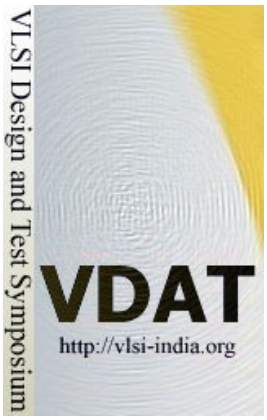
Updated on August 14, 2006



10th IEEE VLSI Design and Test Symposium

VDAT2006

August 9-12, 2006

Venue: International Centre, Goa, India

Sponsored by

VLSI Society of India
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Participants may register for any one of the following tutorials. Tutorial registration is separate from Symposium registration.

Tutorial - I: Analog Design

Analog design in monolithic IC confronts seemingly insurmountable problems due to poor tolerance components and temperature and supply dependant parameters. Further, passive components take up considerable area. The tutorial explains strategies to tackle these problems. These techniques can also be adopted in digital designs for improving yield and reducing power dissipation. The tutorial will be given by two experts in the area – (a) **Prof. KRK Rao**, who is currently with *Texas Instruments India* and was a Professor at IIT Madras before he joined Texas Instruments India, and (b) **Prof. Dinesh Sharma**, a Professor in *the Department of Electrical Engineering at IIT Bombay*.

Tutorial – II: Low Power Electronics and Future Technologies

Power dissipation is a major concern in modern VLSI circuits. The first part of the tutorial, which will be taught by Prof. Vishwani Agrawal of Auburn University, will deal with methods to reduce power dissipation at various levels of abstraction – system-level to gate-level. The second part of the tutorial, which will be taught by **Prof. D. Mukhopadhyay** and **Dr P.K. Basu** of *Jadavpur University*, will consider future technologies that are likely to follow the CMOS technology. The main challenge of nanoelectronics is to exploit quantum behavior and to solve the problems we face: inherent uncertainties and inaccuracies, interconnection problems and the enormous design complexity. Nanoelectronic technology requires an unconventional approach. Although the technology is still in its infancy, time is ripe now to investigate the opportunities for circuits and systems. The tutorial introduces some of the phenomena in nanoelectronics, discuss the device behaviors and to highlight the opportunities that get opened up in the area of integrated circuits and systems. The third part of the tutorial, taught by **C. Venkatesh** of *Indian Institute of Science*, will consider the implementation of capacitors in VLSI with emphasis on MEMS capacitors. Design, analysis, characterization methods and applications will be covered in detail. The theory required for Analysis of Capacitors, Low-frequency Analysis and Applications and High-frequency Analysis and its Applications would be dealt.

Tutorial – III: Testing and Verification

This tutorial consists of two parts. In Part I, which will be delivered by **Baijayanta Ray, Venkataraghavan PK,** and **Sriram Balasubramanian** from *Synopsys, India*, the presenters describe a reliable verification methodology, which ensures low risk while going for first time silicon. This methodology has been successfully applied in developing baseband subsystems for various wireless systems such as GSM, W-CDMA, DAB, MBOA-UWB, and proprietary systems for satellite & terrestrial communication applications. The second part of the tutorial, which will be delivered by **Prof. Indranil Sengupta** of *IIT Kharagpur*, covers the testability issues involved in the design of core based systems. Standardization efforts in this regard will be discussed, with special emphasis on IEEE 1500 standard for embedded core test, CTL, etc.

Advance Program

August 9, 2006, Wednesday

8.00 AM – 9.00 AM	**Breakfast**		
08.30 AM - 09.30 AM	**Registration**		
	Tutorial – I **Venue: MANDOVI** **Analog Design**	**Tutorial – II** **Venue: ZUARI** **Low Power Electronics and Future Technologies**	**Tutorial – III** **Venue: SAL** **Testing and Verification**
09.30 AM - 11.00 AM	**Introduction to Analog Design** ***Prof. K.R.K. Rao***, *Texas Instruments, India, and* ***Prof. Dinesh Sharma***, *IIT Bombay*	**Part I - Low Power Electronics and Systems** ***Prof. Vishwani Agrawal***, *Auburn University*	**Part I - Predictable design and verification flow for wireless systems** ***Baijayanta Ray, P.K. Venkataraghavan*** *and* ***S. Balasubramanian***, *Synopsys*
11.00 AM - 11.30 AM	**Tea Break**		
11.30 AM - 01.00 PM	**Tutorial Continues**	**Tutorial Continues**	**Tutorial Continues**
01.00 PM - 02.00 PM	**Lunch**		
02.00 PM - 03.30 PM	**Tutorial Continues**	**Part II - Beyond CMOS: Problems and Prospects of Nano-electronics** ***D. Mukhopadhyay*** *and* ***P.K. Basu***, *Jadavpur University (2.5 hrs)*	**Part II - Design and Testing Issues in Core Based Systems** ***Indranil Sengupta***, *IIT Kharagpur*
03.30 PM - 04.00 PM	**Tea Break**		
04.00 PM - 06.00 PM	**Tutorial Continues**	**Tutorial Continues** **Part III - MEMS capacitors** ***Venkatesh C***, *Indian Institute of Science, Bangalore (1 hr)*	**Tutorial Continues**
End of Day – 1			

August 10, 2006 – Thursday

Day - 2

VLSI Education Day

08.00 AM – 09.00 AM	**Registration and Breakfast**		
09.00 AM - 09.30 AM	**Inauguration** ***Dr.Shetye**, Director, NIO, Goa* **Inauguration of VSI Goa Chapter** – ***Nitin Konkalekar**, DLINK, Goa*		
09.30 AM - 10.30 AM	**Session 2A-1: Keynote I** **Venue: MANDOVI** ***Prof.M. Balakrishnan**, IIT Delhi* ***Quality VLSI Education: A Dream, Mirage or Reality?***		
10.30 AM - 11.00 AM	**Tea Break**		
11.00 AM - 11.55 AM	**Session-2A-2** **Venue: MANDOVI** **Session Chair: *M. Balakrishnan, IIT Delhi*** Student Projects in **Front-end Design** – Ideas and Execution Challenges **Participants:** Suhas Hiwale, Poseidon Systems, Shankar G.Kambalimath	**Session-2B-2** **Venue: ZUARI** **Session Chair: *D. Mukhopadhyay, Jadavpur University*** Student Projects in **VLSI Physical Design** – Ideas and Execution Challenges **Participants:** Shankar Balachandran, IIT Madras, Rakesh Mehta, Bitmapper, Pune	**Session-2C-2** **Venue: SAL** **Session Chair: *Indranil Sengupta, IIT Kharagpur*** Student Projects in **Verification and Test** – Ideas and Execution Challenges **Participants:** Vishwani Agrawal, C.P. Ravikumar, Nicco Shaleen Bhabu, Cadence
11.55 AM – 12.05 PM	**Break**		
12.05 PM – 01.00 PM	**Session 2A-3** **Venue: MANDOVI** **Short Papers** **Analog Design** **Session Chair: *D. Nagchoudhuri**, DA-IICT*	**Session 2B-3** **Venue: ZUARI** **Short Papers** **Low-power-1** **Session Chair: *Indranil Sengupta,** IIT Kharagpur*	**Session 2C-3** **Venue: SAL** **Short Papers** **Image Processing - 1** **Session Chairs: *M. Balakrishnan**, IIT Delhi and **C.R.Venugopal,** SJCE, Mysore*
	392 P **A Novel Algorithm for Fault Diagnosis in Analog Circuits using Small Change Sensitivity Computation** *Vishal Gupta, ST Microelectronics, **Subash Chandra Bose**, CEERI and Dinesh Jain, Analog Devices*	324 P **Design and Power-Performance Optimization of A Low Leakage Serial CAM** *Niladri Mojumder, D. Mukhopadhyay and **Anup Dandapat**, Jadavpur University*	405 P **Architectural Design and Implementation of a PC based Ultrasound Imaging System** ***Bodhisatwa Mazumdar**, Aman Mediratta, Joydeep Bhattacharyya and Swapna Banerjee, IIT Kharagpur*
	375 P **A Fully On-chip automatic gain control for RF-Transceivers complying IEEE 802.15.4, LR-WPAN** *Harsh T, SIT Lonavala, Abhay N.A, BVP Pune and **Tawade R**, SCOE*	406 P **Design of an Efficient Low Power AES Engine for Zigbee Systems** *Ninad B Kothari, **T.S.B. Sudarshan**, Shipra Bhal, Tejesh.E.C, S. Gururnarayanan, BITS Pilani*	363 P **A Power-Efficient Architecture for the 2-D Discrete Wavelet Transform** ***Rahul Jain,** CoWare India and Preeti Ranjan Panda, IIT Delhi*
	394 P **An Improved Direct Injection Readout Structure for IR FPA** *G.Rajahari, Anil K.Saini, **S.C.Bose** and Chandra Shekhar, CEERI*	245 P **An Energy-Efficient Packet Filtering Architecture for Wireless Sensor Nodes** ***Prashant Sonone** and Saswat Chakrabarti, IIT Kharagpur*	235 P **SOC implementation of the neural network based isolated word recognition** ***V. Amudha**, B.Venkataramani, J.Karthick and C.Praveen, N.I.T, Tiruchirapalli*
			183 P **A Dedicated Processor to Realize Inverse Radon Transform for CT Imaging** ***Abhishek Mitra** and Swapna Banerjee, IIT Kharagpur*
01.00 PM - 02.00 PM	**Lunch**		

Continued…

August 10, 2006 – Thursday

Day - 2

VLSI Education Day - Post-lunch

01.00 PM - 02.00 PM	**Lunch**		
02.00 PM - 03.00 PM	**Session 2A-4** **Venue: MANDOVI** **Short Papers** **Physical Design** **Session Chair: *Vineet Sahula,*** *MNIT Jaipur*	**Session 2B-4** **Venue: ZUARI** **Short Papers** **FPGA Architectures** **Session Chair: *P Sridhar,*** *Controlnet India*	**Session 2C-4** **Venue: SAL** **Custom Design** **Session Chair: *S. Mahant-Shetti,*** *KarMic*
	159 P **Efficient DRC for Verification of Large VLSI Layouts** ***Prosenjit Gupta****, and P.K.Ganesh, IIIT Hyderabad*	340 P **Fault Tolerant FPGA using Redundant Columns** ***Neeraj Goel*** *and Kolin Paul, IIT Delhi*	**Presentation by Participants of the Custom LSI Design Workshop 2006**
	414 P **Cross talk Aware Multi-objective Optimal Routing for Island Style FPGA** *Vineet Sahula, MNIT Jaipur and* ***Rajesh Tiwari****, Texas Instruments India*	384 P **Comparison of Compression techniques for FPGA configuration bit stream** ***Komala Soares****, PCCE, Verna, Goa*	**Blind, but not Color Blind** ***Madhuri Chowdhary***
	Smart Seeder ***Sumit J. Bhat*** **Fun with Faces** ***Sridhar Moorkhandi*** **Sudoku** ***Prashanth Kulkarni***	347 P **FPGA Implementation of a new hardware architecture for Smoothing Two Dimensional Images** ***Narasimhan Venkateswaran****, SVCE, Sriperumbudur and Y.V Ramana Rao, College of Engg, Anna University*	**Audible Colours** *(CLDW06),* ***Vasudha Chourey****, DA-IICT* **Wake-up Fresh Alarm – Part I** ***Shwetha Shanbhag*** **Wake-up Fresh Alarm – Part II** ***Amandeep Singh,*** *Punjab Engineering College (CLDW06)*
03.00 PM - 03.30 PM	**Tea Break**		
03.30 PM - 05.00 PM	**Session 2A-5: Panel Discussion** **Venue: MANDOVI** **Growing and retaining talent in VLSI.** **Panelists: *Anurag Seth,*** *Cadence,* ***Sunit Tyagi****, Intel Tech.,* ***Nagavolu Murty****, Philips,* ***Suhas Hiwale****, Poseidon* **Moderator: *C.P. Ravikumar*** As Indian VLSI panorama expands, getting talent and retaining talent seems to be a major challenge. What is the problem – is it attracting the top students to the VLSI area, offering challenging work, managing the talent, or rewarding the talent? With so many M.Tech programs opening up in Microelectronics and VLSI, it is ironical that companies rarely hire from them and are hunting for talent. Is lack of awareness a problem? Is the quality of education the problem? How can we solve the great talent hunt problem?		
05.00 PM - 05.30 PM	**Tea Break**		
05.30 PM - 06.30 PM	**Session 2A-6** **Venue: MANDOVI** **Short Papers** **Image Processing - 2** **Session Chairs: *M. Balakrishnan,*** *IIT Delhi and* ***C.R.Venugopal,*** *SJCE, Mysore*	**Session 2B-6** **Venue: ZUARI** **Short Papers** **Research Scholars' Forum** **Session Chair: *C.P.Ravikumar,*** *Texas Instruments, India*	**Session 2C-6** **Venue: SAL** **Short Papers** **Technology-1** **Session Chair: *Sunit Tyagi,*** *Intel India*
	367 P **Design and Implementation of Morphological Operations and Median Filter for Image Processing Applications** ***Kapadia Payal Rohit****, Nirma University, Ahmedabad, Raj Singh and Ravi Saini, CEERI*	Research Scholars were invited to present a brief overview on their Ph.D. theses. Experts provided feedback. **Presentations by:** **JVR Ravindra**, IIIT Hyderabad **Ullas Deshmukh**, MNIT Jaipur **B Nagireddy**, Vijayanagar Engg. College **Nidhi Kothari**, BITS Pilani	325 P **Gas Sensor Interface ASIC on 0.7µm CMOS Technology** ***Shobi Bagga****, Navakanta Bhat and S.Mohan, IISc Bangalore*
	124 P **Implementation of MPEG4 Video Decoder on a SoC Multimedia Processor** *Prashanth P, Raghuveer P S, Celstream Technologies, Bangalore, Vinayak A.S. and* ***C.R.Venugopal****, SJCE, Mysore*		387 P **Simulation Of Silicon Nanowire Field Effect Transistors, Carbon Nano Tube Field Effect Transistors and Comparison with Double Gate di-Electric silicon MOSFET** ***E.N.Ganesh****, P.K.Singh, BSA Crescent Engg college, Chennai and Lal Kishore, JNTU Hyderabad*
	137 P **Novel Architecture of Context Modeling for JPEG2000 and a comparison with Taubman's Architecture** ***Pratyush Aditya Kothamasu****, Anand Gautam, A. Geeta Madhuri and Priya Khandelwal, DA-IICT, Gandhinagar*		284 P **Study and Characterization of Gallium Arsenide (GaAs) and Indium Phosphide (InP) Devices for Nanoapplications** ***E.N.Ganesh****, P.K.Singh, BSA Crescent Engg college, Chennai and Lal Kishore, JNTU Hyderabad*

End of Day-2

August 11, 2006 – Friday

Day - 3

08.00 AM - 09.00 AM	**Breakfast**		
09.00 AM - 09.45 AM	**Session 3A-1: Keynote II** **Venue: MANDOVI** ***Rochit Rajsuman**, Advantest* **Future of the ATE** (Open Architecture Tester) **Session Chair: *Navakanta Bhat**, IISc. Bangalore***		
09.45 AM - 10.30 AM	**Session 3A-2: Keynote III** ***Sunit Tyagi**, Intel India* **Intel 65nm technology and 65nm products** **Session Chair: *Navakanta Bhat**, IISc. Bangalore***		
10.30 AM - 11.00 AM	**Tea Break**		
11.00 AM - 01.00 PM	**Session 3A-3** **Venue: MANDOVI** **Robust Design Techniques** **Session Chair: *Sunit Tyagi,** Intel India*	**Session 3B-3** **Venue: ZUARI** **Test–1** **Session Chair: *Vishwani Agrawal**, Auburn University*	**Session 3C-3** **Venue: SAL** **Logic Design** **Session Chair: *V.Kamakoti,** IIT Madras*
	Embedded Tutorial **Design and Analysis of Robust Clock Trees** ***B.G.Madhusudan Rao**, Jagdish Rao, Vish Visvanathan and Udayakumar H, Texas Instruments India (1 hr)*	219 F **Constructing Online Testable Circuits Using Reversible Logic** *Noor Mahammad, Siva Kumar Sastry, Shyam Shroff and **V. Kamakoti**, IIT Madras*	103 F **A Novel Distributed and Interleaved FIFO for Source-synchronous Interconnect** ***Santosh Sood**, Texas Instruments India, Mark Greenstreet and Resve Saleh, University of British Columbia, Canada*
		233 F **Detection of Bridging Fault in Reversible Circuits** *Hafizur Rahaman, **Dipak K. Kole**, Bengal Engg. & Science University, Debesh K. Das, Jadavpur University and Bhargab B. Bhattacharya, ISI Kolkata*	247 F **A Novel all Digital Phase Locked Loop for Phase Tracking in GPS Receivers** *S Moorthi, **K Pavithra**, MIT Campus, Anna University and J Raja Paul Perinbam CEG, Anna University*
	420 T **Embedded Tutorial** **Robust Power Delivery for Sub-100nm Integrated Circuits** *(1 hr)* ***Thenappan Meyyappan**, V Visvanathan, Texas Instruments India and S.K.Nandy, IISc Bangalore*	407 F **On the Quality of Transition Fault Tests** *Jais Abraham, InnoDes Solutions, Bangalore and **Sandeep Jain**, Texas Instruments India*	172 F **RF Energy Scavenging for Wireless Sensor Nodes** *Shantanu Bhalerao, **Abhishek Chaudhary**, Raghavendra Deshmukh and Rajendra Patrikar, VNIT Nagpur*
		412 T **Spectral Characterization of Functional Vectors for Gate-Level Fault Coverage Tests** *Nitin Yogi and Vishwani Agrawal, Auburn University (30 min)*	186 F **High Performance and Area Efficient n-BIT Tree Based Binary Squarer** ***Gopal Paul** and Samir Satpathy, IIT Kharagpur*
01.00 PM - 02.00 PM	**Lunch**		
02.00 PM - 03.00 PM	**Session 3A-4** **Venue: MANDOVI** **Analog Design -2** **Session Chair: *Subhash Chandra Bose**, CEERI***	**Session 3B-4** **Venue: ZUARI** **EDA-1** **Session Chair: *Preeti Ranjan Panda**, IIT Delhi***	**Session 3C-4** **Venue: SAL** **Image Processing-3** **Session Chair: *Aji K.Panda**, NIST Berhampur***
	262 P **Design and Optimization of On-chip Spiral Inductor for Silicon Based RF IC'S** *Genemala Haobijam **and Roy P. Paily, IIT Guwahati***	196 F **Energy Efficient Application Specific Banked Register Files** ***Rakesh Nalluri** and Preeti Ranjan Panda, IIT Delhi*	242 F **Design of Hardware Coprocessor for OTDR Application** ***Ponnmozhi Sampangi** and Nitin Chandrachoodan, IIT Madras*
	326 F **General Purpose Capacitive Sensing Circuit using Correlated Double sampling** *Sandeep K, **Chaitanya K** and Navakanta Bhat, IISc, Bangalore*	374 F **Exact Method for Estimating Expected Settling Power in Sequential Circuits** ***Diganchal Chakraborty**, P.P.Chakrabarti and Pallab Dasgupta, IIT Kharagpur*	359 F **An efficient FPGA Implementation of a Cryptographic Hash Algorithm Based on Cellular Automata** ***Roshni Chatterjee** and Dipanwita RoyChowdhury, IIT Kharagpur*
	371 F **A Novel LO circuit for Sub-Harmonic Mixer** ***R.N.Biswas**, C.Parikh, DA-IICT and G.P.Krishna Kishore, ATLAB Inc, Korea*	329 F **Critical Path modeling for Dynamic Voltage Scaling (DVS) in Low Power Applications** ***Bishnu Prasad Das**, Bharadwaj Amrutur and H.S. Jamadagni, CEDT, IISc Bangalore*	333 F **Design & Study of an Electrostatic Torsion Micro Actuator for Beam Steering in Horizontal Plane** ***D. Vijaya Bhargava** and Roy P. Paily, IIT Guwahati*
	128 P **Highly Linear, Highly Efficient Power Amplifier Design Using Diode Nonlinear Capacitance** ***Mrunal. A.K.**, IITB, Makarand Shirasgaonkar, Qualcore Logic Ltd, Hyderabad and Rajendra Patrikar, VNIT, Nagpur*	379 P **Waveform Analysis and Delay Prediction for CMOS driven RLC-Modeled VLSI Interconnect** ***B.K.Kaushik**, IIT Roorkee, S.Sarkar, Modi Inst. of Tech. & Sc., Sikar and R.P.Agarwal*	356 F **A Novel Low Power Bus Encoding Technique for Minimizing RGB Transitions for LCD Display of Digital Camera** ***J.V.R. Ravindra**, K.S. Sainarayanan and M.B. Srinivas, IIIT, Hyderabad*
03.00 PM - 03.30 PM	**Tea Break**		

August 11, 2006 – Friday

Day – 3 - Post-lunch

03.00 PM - 03.30 PM	**Tea Break**		
03.30 PM - 04.30 PM	**Session 3A-5: Keynote IV** **Venue: MANDOVI** **Dipu Pramanik**, Group Director, TCAD DFM products, Synopsys **Impact of layout on variability of devices for sub 90nm Technologies** **Session Chair: *C.P.Ravikumar***		
04.30 PM - 05.30 PM	**Session 3A-6** **Venue: MANDOVI** **Physical Design - 1** **Session Chair: *Pavan Kumar Gunupudi,* Carleton University**	**Session 3B-6** **Venue: ZUARI** **Test - 2** **Session Chair: *Vishwani Agrawal,* Auburn University**	**Session 3C-6** **Venue: SAL** **Proposals for VSI Events** **Session Chair: *C.P.Ravikumar,* Texas Instruments India**
	107 F **Handling Trapezoidal Conductor Cross-sections in a Statistical Capacitance Extractor** ***Subramanian Rajagopalan*** *and Shabbir Batterywala, Synopsys India*	267 P **A Novel Unified Framework for Functional Verification of Processors Using Constraint Solvers** *Debi Prasad, Archna Rai, Karthik V., Senthil Kumar,* ***V. Kamakoti****, IIT Madras, Kailasnath S. and Vivekanada Vedula, Intel Corporation, Austin*	**Proposals for VSI Events can be brought to this forum.** Please send the proposals by filling out a form at VSI Sponsorship Page. You will be given an opportunity to present the details of the program at this forum.
	322 F **A Novel CMOS Compatible Three Terminal 3D Tunable Micro Inductor** ***V. Siva Rama Krishna****, K.Jayant and Navakanta Bhat, IISc Bangalore*	158 F **Automatic Test Generation for Temporal Coverage Points Using a Stochastic Tree Model** *Anindyasundar Nandi,* ***Bhaskar Pal****, Pallab Dasgupta and Partha P. Chakrabarti, IIT Kharagpur*	
	425 F **Integrated Stability Analysis Methods for Hybrid Systems** ***S. Jairam****, Texas Instruments India and Navakanta Bhat, IISc Bangalore*	216 F **Detecting Faults at the Time They Occur** *Abhijeet Kumar,* ***Sayantan Das****, Pallab Dasgupta and P. P. Chakrabarti, IIT Kharagpur*	
05.30 PM - 06.00 PM	**Tea Break**		
06.00 PM - 07.00 PM	**Venue: MANDOVI** **Banquet Talk**		
7.00 PM – 8.30 PM	**Banquet Dinner**		
End of Day - 3			

August 12, 2006 – Saturday

Day - 4

08.00 AM - 09.00 AM	**Breakfast**
09.00 AM - 09.30 AM	**Registration**
09.30 AM - 10.30 AM	**Session 4A-1: Keynote V** **Venue: MANDOVI** **Nagaraj N.S.**, *Texas Instruments India* **Future of Interconnect in Nanometer Area** **Session Chair: *C.P.Ravikumar***
10.30 AM - 11.00 AM	**Tea Break**
11.00 AM - 12.30 PM	**Session 4A-2: Panel II** **Venue: MANDOVI** **VLSI - How long will "Advantage India" last?** **Panelists: *Shyamal Datta,* Cadence, *Nagvolu Murty,* Philips Moderator: *C.P. Ravikumar*** In the last few years, India has become the favored nation for expansion for many multinational semiconductor/VLSI companies. Several startups have also bloomed in this segment in the past few years. However, will this trend continue? Is outsourcing to India a profitable venture? What threats do we face from other competing nations in this segment? Have we got our act together?
12.30 PM – 1.30 PM	**Lunch**
End of Symposium	

Information

*Please watch updates on VDAT at http://vlsi-india.org/ The idea behind the VLSI Design And Test (VDAT) Symposium is to promote Research and Development on all aspects of VLSI in India. This symposium is a forum for free discussion of hot and emerging topics in VLSI. It provides a meeting place for VLSI professionals working in India and abroad. We have been holding this event since 1998, and the participation in the event has steadily gone up every year. Until 2004, the event was called "**VLSI Design and Test Workshops**." The VLSI Industry in India and academic community working in the area of VLSI has provided immense support to the symposium.*

*VDAT is sponsored by the **VLSI Society of India**. Please consult http://vlsi-india.org/vsi for more information on VSI"s mission and goals. If you are unable to download the page, please send mail to vsiaccounts@vlsi-india.org for a softcopy of the application form.*

Consult http://vlsi-india.org/vsi/activities/ for updates on the activities of the VLSI Society of India. If you wish to become a member of the VLSI Society of India, you can download the form from http://vlsi-india.org/vsi/membership/.

Accommodation

A limited accommodation for students is planned at the **Goa University Guesthouse**. And a limited number of rooms are available for other participants at the **Goa International Centre** (http://www.internationalcentregoa.com/) Details available from our website http://vlsi-india.org

Also from our Download section http://203.200.181.210/index.php?dir=

Symposium Committee

General Co-Chairs

C.P. Ravikumar, Texas Instruments India
P. Sridhar, Controlnet India

Venue:
The International centre
Goa University Road
Dona Paula, Goa - 403 004

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History of VDAT:

Event	Venue	Date	Participants
1st VDAT	Chennai	January 7, 1998	30
2nd VDAT	New Delhi	August 6-7, 1998	70
3rd VDAT	New Delhi	August 20-21, 1999	120
4th VDAT	New Delhi	August 25-26, 2000	150
5th VDAT	Bangalore	August 16-18, 2001	220
6th VDAT	Bangalore	August 29-31, 2002	300
7th VDAT	Bangalore	August 28-30, 2003	300
8th VDAT	Mysore	August 26-28, 2004	250
9th VDAT	Bangalore	August 10-13, 2005	320

INTERNATIONAL CENTRE GOA

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Registration Information:

- Registration permits you to participate in all the Technical sessions and Tutorials organized as part of the Symposium, and includes refreshments and lunch on all days.
- Please send your registration fee through a draft made out to "*VLSI Design and Test Symposium, 2006",* payable at Bangalore*.*
- The draft must be sent to *Mr.Gopal Naidu, Finance Chair (VDAT 2006), Texas Instruments India, Bagmane Tech Park, C.V. Raman Nagar, Bangalore 560093*.
- If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Foreign Currency or Credit Card payments.
- The current exchange rate is approximately 1 US dollar = 45 Indian rupees.
- Even those of you who plat to register on the spot are requested to communicate your desire to attend VDAT 2006 to vdat06@hotmail.com with details of vehicle registration number (if any) and laptop number (if any). Without this, you may face difficulties during registration. Please mark the subject line of the mail as "Vehicle No." or "Laptop No."
- If you are registering for a tutorial, indicate the first and second preference of the tutorial. There are limited seats in each tutorial. If we cannot register you in the tutorial of your choice, we will refund the amount.
- A processing fee of Rs.500/- will be applied against all cancellations.

Symposium Registration Amount

	Fellow	Indian Faculty/ Student	Indian Industry VSI/ IEEE Member	All Foreign Participants	Others
Before June 30, 2006	Rs.1500/=	Rs.2500/=	Rs.6000/=	US$ 150.00	Rs.7000/=
After June 30, 2006	N/A	Rs.3000/=	Rs.7000/=	US$ 200.00	Rs.8000/=

Tutorial Registration Amount

Before June 30, 2006	Rs.1000/=	Rs.1500/=	Rs.2000/=	US$ 100.00	Rs.2500/=
After June 30, 2006	Rs.1500/=	Rs.2000/=	Rs.2500/=	US$ 125.00	Rs.3000/=

At the rear side of DD, mention the choice of Tutorial Title: T1, T2 or T3

Correspondence address for Registration:

Mr. Gopal Naidu
Finance Chair, VDAT2006
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park, Opp. LRDE
C.V.Raman Nagar, Bangalore – 560 093
FAX: 91-80-25048213
vdat06-regn@hotmail.com

Venue Information:

The venue of the Symposium is the International Center, located at the tranquil Dona Paula, near Goa University.

Please send mail to vdat06@hotmail.com and inform your vehicle's registration number and Laptop number if you will come in your private vehicle and/or bring your laptop.

Information on Hotels at Goa and Travel details are available from our site and the download section. ***Please plan your travel***.

During August, Goa witnesses monsoon, and hence protective gears suggested.

International Centre, Goa (ICG) is a non-profit Institutional Society, which provides a stimulating environment for generation of ideas, a fertile ground for appreciating beauty in all cultures and an ambience for relaxation.

VSI Membership Form

(For New membership and renewals)

VLSI Society of India

http://vlsi-india.org/vsi/

Registered Society under KSR Act 1960, Rule 1961

E-mail: **vsiaccounts@vlsi-india.org**, **vsisecy@vlsi-india.org**

New Members to affix photograph.

1. Existing Membership No: ☐☐☐☐ (Quote additional Old No. If any): ☐☐☐☐

Member (tick as applicable): ☐ **Student** / ☐ **Non-student** / ☐ **Corporate**

2. Your Name:

3. Your Profession/ Designation:

4. Your e-mail address:

5. Your Contact address:

6. Your Professional address (if different from above):

7. Your Area of specialization:

8. Would you like to review papers in events organized by VSI? :

9. How many papers are you willing to review? :

10. Your Brief bio-data: Attach separately

11. How can you contribute to the activities of VSI? :

12. What Activities would you like VSI to organize? :

13. Details of Payment:

Cash	
DD no:	
Dated:	
Drawn on Bank:	
Amount:	

I agree to be a member of the VLSI Society of India and have read and understood the charter of the society. I will actively contribute towards the objectives of the society.

Place and Date: **Member Signature**

Category	**Membership Rates:**	
	Yearly	**5-yearly**
Student Member:	Rs. 500/=	N/A
Non-student member:	Rs. 1,000/=	Rs 4,500/-
Corporate member:	Rs. 10,000/=	Rs 45,000/-

Mail the form along with the DD and biodata to:
Mr. Gopal Naidu
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park, Adjacent to LRDE, C.V.Raman Nagar
Bangalore: 560 093 **(FAX: 91-80-25048213 Attn: VSI Accounts)**

The DD to be made out to: "VLSI Society of India" and payable at Bangalore.

- Please write "**Towards VSI Membership - New/ Renewal**" at the rear side of DD.
- The same form to be used for a new membership or Renewal.
- Students to attach college credentials.
- Processing the card subject to the DD receipt. Please allow two weeks.
- Write to **vsiaccounts@vlsi-india.org** with details of payment and copy to **vsisecy@vlsi-india.org** to speed up the process.
- The photograph is for official records only and will not be imaged onto the membership card.
- In the event of change of address, please intimate.