# 9th IEEE VLSI Design and Test Symposium

**August 10-13, 2005**

**Venue: Learning Center, Wipro Campus, Electronics City, Bangalore, India**

VDAT

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| Advance Program for August 10, 2005 (Wednesday) - Day-1 | | |
|---|---|---|
| 8.30 – 9.30 AM | **Registration** | |
| | **Session 1A: Tutorial – I**<br><br>***Analog Design and Synthesis Issues for Scaling CMOS Technologies***<br><br>**Speakers: Dinesh Sharma**, IIT Bombay, **Chetan Parikh**, DA-IICT, and **Ranga Vemuri**, University of Cincinnati<br><br>**Venue: Room-Coral** | **Session 1B: Tutorial – II**<br><br>***Implementation Challenges in Embedded Systems***<br><br>**Speakers: Ajit Rao**, TI India<br>**Mani Manoharan**, Wipro, **Indrajith Radhakrishnan**, Wipro, **Sadashivan Manickam**, Wipro<br>**Pradeep Ganesh Natarajan**, Wipro<br>**Coordinator: Arvind Chauhan**, Wipro<br><br>**Venue: Room-Dolphin** |
| 9.30 AM – 11.00 AM | **Tutorial** | **Tutorial** |
| 11.00 AM – 11.30 AM | Tea Break | |
| 11.30 AM – 1.00 PM | **Tutorial Continues** | **Tutorial Continues** |
| 1.00 PM – 2.00 PM | Lunch | |
| 2.00 – 3.30 PM | **Tutorial Continues** | **Tutorial Continues** |
| 3.30 PM – 4.00 PM | Tea Break | |
| 4.00 PM – 6.00 PM | **Tutorial Continues** | **Tutorial Continues** |
| **End of Day-1** | | |

***Tutorial – I:*** **Analog Design and Synthesis Issues for Scaling CMOS Technologies**
**Speakers: Dinesh Sharma**, IIT Bombay, **Chetan Parikh**, DA-IICT and **Ranga Vemuri**, University of Cincinnati

As device dimensions and operating voltages are scaled down, conventional approaches to the design of analog circuits have to be modified. This tutorial will present a review of some major techniques used in analog circuit design for low-voltage applications. The CMOS amplifier will be the focus of the tutorial, although many of the techniques described will be applicable for a variety of analog circuits. The topics covered in the tutorial are:

- Brief review of conventional CMOS amplifier design
- Relationship between the transistor parameters and biases, and amplifier performance; basic design techniques.
- Low-power design - Rail-to-rail amplifier architectures, feedback techniques, and current source/mirror architectures.
- Analog Circuit Synthesis – sizing, layout synthesis, topology selection/generation, performance closure
- Overview of synthesis techniques
- Analog performance modeling – macro models and symbolic models
- Layout-inclusive synthesis models – parasitic estimation, layout sampling, convergence and efficiency

*The speakers are well known personalities in Analog design and synthesis domain. More details of the tutorial and biographies of the speakers are available from the VDAT website – http://vlsi-india.net*

***Tutorial – II: Implementation Challenges in Embedded Systems***
**Speakers: Ajit Rao**, TI India, **Mani Manoharan**, Wipro**, Indrajith Radhakrishnan**, Wipro, **Sadashivan Manickam**, Wipro
**Pradeep Ganesh Natarajan**, Wipro.
**Coordinator: Arvind Chauhan**, Wipro

*This tutorial will discuss the challenges in development of Embedded Systems. The topics covered in the tutorial include:*

- Porting Embedded Linux for an ARM based system - Key Kernel elements to be ported, Porting Steps and Debugging, Ensuring Stability and Stress Testing
- USB Software Stack Development for Embedded Systems - USB Software Components, Key System Resource Requirements, USB Stack Implementation for Embedded Linux
- HW/SW Partitioning - Design Decisions, Tools and Techniques
- HW/SW Cosimulation - SoC HW-SW Design Constraints, Need for Cosimulation, Tools and Techniques, Example

*The speakers are expert practicing professionals in the area of Embedded Systems. More details of the tutorial and biographies of the speakers are available from the VDAT website – http://vlsi-india.net*

*Please watch the VDAT website or follow the vdat@yahoogroups.com mailing list for any updates to the program. Since the space for tutorials is limited, we may be forced to shortlist participants. If we are unable to register you, you will be intimated by e-mail, and a refund will be made by the VLSI Society of India.*

| Advance Program for August 11, 2005 (Thursday) - Day-2<br>VLSI Education Day | | | |
|---|---|---|---|
| 8.00 AM - 9.00 AM | **Registration** | | |
| 9.00 AM - 9.30 AM | **Inauguration** | | |
| 9.30 AM - 10.30 AM | **Session 2A-1: Keynote Talk**<br>**Bobby Mitra**, Texas Instruments: ***VLSI Education in India***<br>**Venue: Room-Coral** | | |
| 10.30 - 11.00 AM | Tea Break | | |
| 11.00 AM - 1.00 PM | **Session 2A-2: Workshop: *Taking Student Projects to Silicon***<br>**Speakers:**<br>**Dinesh Sharma**, IIT Bombay, **Debashis Dutta**, MCIT, **M.J. Zarabi**, SCL Chandigarh and **Satya Gupta**, Open Silicon<br>**Moderator: C.P. Ravikumar,** Texas Instruments, India<br>**Venue: Room-Coral** | | |
| 1.00 PM - 2.00 PM | Lunch | | |
| | **Session-2A-3**<br>**Moderator: Taher Abbasi**, Cadence<br>**Venue: Room-Coral** | **Session 2B-3**<br>**Moderator: Gopal Krishna**, Advance Micro Devices<br>**Venue: Room-Mermaid** | **Session 2C-3**<br>**Moderator: Jayanta Lahiri**, Alliance Semiconductors<br>**Venue: Room-Dolphin** |
| 2.00 - 3.30 PM | **Student Projects in Front-end Design – Ideas and Execution Challenges**<br>**Participants: M. Balakrishnan**, IIT Delhi, **V. Kamakoti**, IIT Madras, **S. Karthik**, Analog Devices, **Karthik Madathil**, Texas Instruments<br>*Experts will lead discussion groups to come up with project ideas, which will be hosted on VSI/ISA websites.* | **Student Projects in VLSI Physical Design – Ideas and Execution Challenges**<br>**Participants: G.S. Visweswaran**, IIT Delhi, **Anand Anandkumar**, Magma, **Shabbir Batterywala**, Synopsys, **Navakanta Bhat**, IISc, Bangalore<br>*Experts will lead discussion groups to come up with project ideas that will be hosted on VSI/ISA websites.* | **Student Projects in Verification and Test – Ideas and Execution Challenges**<br>**Participants: Pallab Dasgupta**, IIT Kharagpur, **R. Parekhji**, Texas Instruments, **Subir Roy**, TI India, **Vishwani Agrawal**, Auburn University<br>*Experts will lead projects to come up with ideas that will be hosted on VSI/ISA websites.* |
| 3.30 – 4.00 PM | Tea Break | | |
| 4.00 – 5.30 PM | **Session 2A-4: Panel Discussion**<br>**Topic: The Role of Industry in VLSI Education**<br>**Moderator: C.P. Ravikumar**<br>*While industry complains about the quality of education in VLSI and allied subjects, academicians are quick to point out the need for the industry to do something about it. The panel will discuss what role the Indian VLSI industry could, should, and would play in the coming years.*<br>**Panelists: P.P. Das**, Interra Systems, **H.V. Ananda**, Synplicity, **P.P. Chakrabarti**, IIT Kharagpur<br>**Venue: Room-Coral** | | |
| 5.30 PM - 6.00 PM | Break | | |
| 6.00 PM - 7.00 PM | **Session 2A-5**<br>**Poster Papers**<br>**Applications – I**<br>**Chair: B. Venkataramani**, NIT Trichy<br>**Venue: Room-Coral** | **Session 2B-5**<br>**Poster Papers**<br>**Circuits and Devices**<br>**Chair: D. Nagchoudhuri**, DA-IICT<br>**Venue: Room-Mermaid** | **Session 2C-5**<br>**Poster Papers**<br>**EDA – I**<br>**Chair: Vineet Sahula**, MNIT<br>**Venue: Room-Dolphin** |
| | **P. Jagadesh**, G. Elangovan and P. Vanajaranjan, College of Engineering, Anna university<br>*SoC Implementation for Hearing Aid Noise Recognizer* | **H. Mangalam,** S. Subramanian, Sri Krishna College of Engg. & Tech., Coimbatore and K. Gunavathi, G. Prabhu, PSG College of Engineering, Coimbatore<br>*Domino Logic with Variable Body Biased Keeper* | **Aruleswari G** and V.Lakshmi prabha, Government College of Technology, Coimbatore<br>*An Adaptive Algorithm for power management at system level* |
| | **KDNVS Prasad**, Rajeeva G.K. and M. Jain, Central Research Laboratory, BEL<br>*A Generic Time Division Duplex Scheme for Synchronous Traffic and Control of Remote Communication Devices* | **P. Vijaykumar**, M. Santhanalakshmi and K. Gunavathi, PSG College of Technology, Coimbatore<br>*Efficient Energy Recovery Technique for Positive Feedback Adiabatic Logic* | **S. Mandal**, A. Somani, J. Agarwal, S. Sural and A. Patra, IIT Kharagpur<br>*Crosstalk aware Line Search Algorithm for Analog Routing* |
| | **S.R. Chowdhury** and H. Saha, Jadavpur University, Kolkata<br>*VHDL Model of a Cognitive System for Telemedicine Applications* | **A.A. Prasad**, D. Datta, S. Ganguly and S. Dasgupta**,** Indian School of Mines, Dhanbad<br>*Extraction of Gate Tunneling Current in Gaussian Doped High-k Ultra-Thin-Body Double Gate (DG) MOSFET* | **J.V.R. Ravindra,** K.S. Sainarayanan and M.B. Srinivas, International Institute of Information Techonology, Hyderabad<br>*A Novel Bus Coding Technique for Low Power Data Transmission* |
| | **Samir Roy**, National Institute of Technical Teachers' Training & Research, West Bengal<br>*A Universal Logic for Quantum-Dot Cellular Automata* | **Lalitha G.**, A. Garimella, Laura Escobedo and Jaime Ramirez-Angulo, New Mexico State University, USA<br>*Compact Low Voltage VHF Continuous –Time Current Mode Filters Based on First Order Low-Pass Building Blocks* | S. Chattopadhyay, IIT Kharagpur, H. Agarwal and **M. Chawla**, IIT Guwahati<br>*Evolving Cellular Automata for Low power Testing of Circuits* |
| | **Sahil M. Bansal**, Punjab Engineering College and D.Nagchaudhuri, DA-IICT<br>*Minimization in Variation of Output Characteristics of a SOI MOS Due to Self Heating* | | |
| **End of Day-2** | | | |

| Advance Program for August 12, 2005 (Friday) - Day-3 | | | |
|---|---|---|---|
| 9.00 AM - 9.30 AM | **Registration** | | |
| 9.30 AM - 10.30 AM | **Session 3A-1: Keynote Talk**<br>**Speaker: Ramesh Emani**, Wipro Technologies:<br>***Design Going Global: Implications and Lessons***<br>**Chair: Nagaraj Subramanyam**, Texas Instruments<br>**Venue: Room-Coral** | | |
| 10.30 AM - 11.00 AM | Tea Break | | |
| 11.00 AM - 12.00 PM | **Session 3A-2: Keynote Talk**<br>**Speaker: T.W. Williams,** Synopsys<br>***Design For Testability – What is it and How did we get here?***<br>**Chair: C.P. Ravikumar**, Texas Instruments, India<br>**Venue: Room-Coral** | | |
| 12.00 PM - 1.00 PM | **Session 3A-3**<br>**Design Techniques – I**<br>**Chair: G. S. Visweswaran**, IIT Delhi<br>**Venue: Room-Coral** | **Session 3B-3**<br>**Low Power – I**<br>**Chair: Navakanta Bhat**, IISc, Bangalore<br>**Venue: Room-Mermaid** | **Session 3C-3**<br>**EDA – II**<br>**Chair: Partha Ray**, National Semiconductor<br>**Venue: Room-Dolphin** |
| | **K.K. Muralidharan**, Wipro Technologies<br>*Mixed design of Self-Timed Logic in Synchronous Systems*<br>**Embedded Tutorial** | **S. Sarkar** and Subash Chandar G., Texas Instruments India<br>*Low Power Techniques for CMOS Designs*<br>**Embedded Tutorial** | **H. Rahaman** Bengal Engg. College, D.K. Das, Jadavpur University, and B.B. Bhattacharya, IIT Kharagpur<br>*Synthesis and Testing of Reversible Logic – A Survey*<br>**Embedded Tutorial** |
| | **A. Chaudhary**, G. Gupta and M. Balakrishnan, IIT Delhi<br>*Factoring Large Numbers using FPGA* | Siri Uppalapati, GDA Technologies, Inc., USA, Michael L. Bushnell, Rutgers University and **V.D. Agrawal**, Auburn University<br>*Glitch-Free Design of Low Power ASICs using Customized Resistive Feedthrough Cells* | **S. Mandal**, Soumya P., A. Somani, S. Sural and A. Patra IIT Kharagpur<br>*UML based Object Oriented Methodology for Analog Test Structure Design Automation* |
| 1.00 PM - 2.00 PM | Lunch | | |
| 2.00 PM - 3.00 PM | **Session 3A-4**<br>**Low Power – II**<br>**Chair: P.V. Anandmohan**, ECIL<br>**Venue: Room-Coral** | **Session 3B-4**<br>**Applications – II**<br>**Chair: P.R. Panda**, IIT Delhi<br>**Venue: Room-Mermaid** | **Session 3C-4**<br>**EDA – III**<br>**Chair: M. Balakrishnan**, IIT Delhi<br>**Venue: Room-Dolphin** |
| | **A.P. James** and Ajayan K.R., College of Engineering, Trivandrum<br>*Nanoscale design of Low power Supply Pseudo Resistive Cascode Current Mirror* | **D. Mukhopadhyay** and Dipanwita R.C., IIT Kharagpur<br>*Programmable Galois Multiplier Using Cellular Automaton* | **B. Sarker,** Cadence Design Systems<br>*Petri Net Modeling of GALS and Implementation in Baseband Datapath component of an IEEE 802.11a compliant modem* |
| | **R. Paul**, A. Patra and S. Mukhopadhay, IIT Kharagpur<br>*Verilog - A Modeling of Parasitic and Biasing effects in PSRR behavior of Brokaw Bandgap Voltage Reference* | **G.S. Nim**, B.S. Chauhan and A. Thapliyal, IRDE, Dehradun<br>*Real-Time Image Processing System* | **A. Sarkar,** P.P. Chakrabarti and Rajeev K., IIT Kharagpur<br>*Boundary Fair Round-Robin: A Fast Fair Scheduler* |
| | V. Lakshmi Prabha, **K. Balamurugan**, GCT, Coimbatore and Elwin C.M., Government college of Engineering, Vellore<br>*Online Adaptive Power Management for Non-Stationary Service Request* | **H. Dhand**, N.Goel, M.Agarwal and K.Paul, IIT Delhi<br>*Partial and Dynamic Reconfiguration in Xilinx FPGAs – A Quantitative Study* | **S. Chatterjee**, P.P. Chakrabarti and Rajeev K., IIT Kharagpur<br>*An Optimal Algorithm for Register Renaming: A Post Compilation Technique* |
| 3.00 PM - 3.30 PM | Tea Break | | |
| 3.30 PM – 4.30 PM | **Session 3A-5: Keynote Talk**<br>**Speaker:** Kaushik Roy, Purdue University. ***Advances in Low Power Design Techniques***<br>**Chair: Bharadwaj Amruthur**, Indian Institute of Science<br>**Venue: Room-Coral** | | |
| 4.30 PM - 5.30 PM | **Session 3A-6: Invited Talk**<br>**Chair: Vishwani Agrawal**, Auburn University<br>**Speaker: Nilanjan Mukherjee**, Mentor Graphics Corporation, USA.<br>*Test Quality Challenges in the Nanometer Era*<br>**Venue: Room-Coral** | **Session 3B-6: Invited Talk**<br>**Chair: Dinesh Sharma**, IIT Bombay<br>**Speaker: Ashok Balivada**, Analog Devices, India.<br>*Signal Integrity and Analysis*<br>**Venue: Room-Mermaid** | **Session 3C-6: Invited Talk**<br>**Chair: Shabbir Batterywala**, Synopsys<br>**Speaker: Susmita Sur-Kolay**, Indian Statistical Institute<br>*Advances in Physical Design Automation*<br>**Venue: Room-Dolphin** |
| 5.30 PM - 6.00 PM | Break | | |
| 6.00 PM - 7.00 PM | **Session 3A-7**<br>**Poster Papers**<br>**Testing – I**<br>**Chair: Bhargab Bhattacharya**, ISI Calcutta<br>**Venue: Room-Coral** | **Session 3B-7**<br>**Poster Papers**<br>**Synthesis**<br>**Chair: Anantha Bhat**, Synopsys<br>**Venue: Room-Mermaid** | **Session 3C-7**<br>**Poster Papers**<br>**Applications – III**<br>**Chair: V. Kamakoti**, IIT Madras<br>**Venue: Room-Dolphin** |
| | **S.K. Nathappan**, M.V. Raghavulu and Vanathi P.T., PSG College of Technology, Coimbatore<br>*CMOS SRAM Fault Detection Using Dynamic Power Supply Current* | **S. Saha,** IIT Roorkee, S. Sarkar and S. Sur-Kolay, Indian Statistical Institute<br>*Comparative study of Logic Synthesis Objectives in FPGA Design Flow* | **M.A. Khan** and Y.P. Singh, CDAC, Noida<br>*Omura's Modular Addition for FPGA Implementation of IDEA Cipher Block* |
| | **D. Mukhopadhyay** and N.N. Mojumder, Jadavpur University<br>*Energy-Performance Improvement of Content Addressable Memory by Dual-Threshold CMOS Technology* | **M.S. Bhat**, Rekha S. and H.S. Jamadagni, CEDT, IISc, Bangalore<br>*Synthesis of Multiple-Valued Arithmetic Functions using Evolutionary Process* | **Naveen H.N.** and N.Shekar V.Shet, NITK, Surathkal<br>*Performance optimized VLSI Implementation of RC5 Encryption Algorithm* |
| | **Seema B.**, Thapar Institute of Engineeing & Technology, Patiala and G.K. Sharma, IT Group, IITM, Gwalior<br>*Search Space Pruning for Faster Test Generation based on Parallel and Adaptive GA* | **A. Bhasin**, S. Arora and M. Ameria, HCL Technologies, Noida<br>*Enabling ESL Design Through Behavioral Synthesis* | S. Anandh, L.Karthick, **L. Ponnambalam**, S. Rajaram and V.Abhaikumar Thiagarajar College of Engineering, Madhurai<br>*FPGA Implementation of OFDM WLAN Modem* |
| 7.00 PM – 8.30 PM | **Banquet Dinner** | | |
| **End of Day-3** | | | |

| Advance Program for August 13, 2005 (Saturday) - Day-4 | | | |
|---|---|---|---|
| 9.00 AM - 9.30 AM | **Registration** | | |
| 9.30 AM - 10.30 AM | **Session 4A-1: Keynote Talk**<br>**Speaker**: **Sumeet Agarwal**, Mobility Group, Intel: **Power management**<br>**Chair: V. Visvanathan**, Texas Instruments<br>**Venue: Room-Coral** | | |
| 10.30 AM - 11.00 AM | Tea Break | | |
| 11.00 AM - 12.00 PM | **Session 4A-2**<br>**Testing – II**<br>**Chair: Ram Jonnavithula**, Texas Instruments India<br>**Venue: Room-Coral** | **Session 4B-2**<br>**Memory Design**<br>**Chair: Jayanta Lahiri**, Alliance Semiconductors<br>**Venue: Room-Mermaid** | **Session 4C-2**<br>**Architecture**<br>**Chair: Ravi Koodli**, Infineon<br>**Venue: Room-Dolphin** |
| | **Thakur S. K.**, A. N. Chandorkar, IIT Bombay and R.A. Parekhji, TI India<br>*Diagnostic Testing of Memories for Static and Dynamic Faults* | **A.S. Kothari,** Purplevision Technologies<br>*Area Optimization Tips in Memory BIST* | P.R. Panda**,** IIT Delhi and **Viresh Kumar**, Infineon<br>*A technique for predicting the effect of Data Cache Associativity* |
| | **P. Basu**, S. Das, A. Banerjee, P. Dasgupta and P.P. Chakrabarti, IIT Kharagpur<br>*Test Plan Coverage by Formal Property Verification* | **A.S. Mudlapur**, Vishwani Agrawal, and Adit Singh. Auburn University,<br>*A Novel Random Access Scan Flip-Flop Design* | **C. Karfa**, J.S. Reddy, S. Biswas, C.R. Mandal, D. Sarkar, IIT Kharagpur<br>*SAST: An Interconnection Aware High-level Synthesis Tool* |
| | **S. Banerjee** and Dipanwita R.C., IIT Kharagpur<br>*An Integrated Computer Aided Test (CAT) Tool for System on Chip* | **Vasudha G.** and Rengarajan K., Texas Instruments India<br>*An Accurate Critical Path Based Characterization Scheme for Memory Compilers* | **S. Bhanja** and Thara Rejimon, University of South Florida<br>*Probabilistic Error Model for Unreliable Nano-logic Gates* |
| 12.00 PM - 1.00 PM | **Session 4A-3**<br>**VSI – The Road Ahead**<br>**Chair: C.P. Ravikumar**<br>**Venue: Room-Coral** | **Session 4B-3**<br>**Analog Design**<br>**Chair: Shanti Pavan**, IIT Madras<br>**Venue: Room-Mermaid** | **Session 4C-3**<br>**DSP**<br>**Chair: Nitin Chandrachoodan**, IIT Madras<br>**Venue: Room-Dolphin** |
| | The calendar of VLSI Society of India for 2006 is under construction. Proposals for holding events of VSI are invited. Brief reports from workshops held in 2005 will be presented by respective organizers. If you wish to hold a workshop on a specific topic, please write to ravikumar@vlsi-india.net. You will be invited to make a brief presentation about the event, including the title of the workshop, its intent, expected outcome, and budget. You can download the appropriate form from http://vlsi-india.net to help you with the planning. | S. Moghe, **S. Biswas**, J.K. Agrawal, D. Sarkar, S. Mukhopadhyay and A. Patra, IIT Kharagpur<br>*A Hybrid System Approach to Failure Diagnosis of Analog VLSI Circuits: A Case Study of DC-DC Buck Converters* | **N.J.R. Muniraj**, Sona College of Technology and R.S.D.Wahida Banu, Government College of Engg, Salem<br>*On ways to improve the Adaptive Filter Technique using Verilog HDL and CPLD* |
| | | Uday Goel, Sachit Grover and **G.S. Visweswaran**, IIT Delhi<br>*Low Voltage Current Mode Pipelined Analog to Digital Converter* | G. Seetharaman, **B. Venkataramani** and G. Lakshminarayanan, NIT, Tiruchirappalli<br>*Design and FPGA Implementation of Wavepipelined Image Block Encoders using 2D-DWT* |
| | | **K.S.R.K. Prasad**, N. Suresh and B. Swapna , N.I.T., Warangal<br>*A 1.2V Low Power CMOS Bulk Driven Operational Amplifier* | **Satyendra K.**, K.S Ramesh, Anbuselvi J. and S.R. Choudhury, Central Research Laboratory, BEL<br>*FPGA Implementation Of Soft Decision Viterbi Decoder* |
| 1.00 PM - 2.00 PM | Lunch | | |
| 2.00 PM - 3.30 PM | **Session 4A-4**<br>**Verification**<br>**Chair: Subir Roy**, Texas Instruments India<br>**Venue: Room-Coral** | **Session 4B-4**<br>**Design Techniques – II**<br>**Chair: S.K. Nandy**, Indian Institute of Science<br>**Venue: Room-Mermaid** | **Session 4C-4**<br>**Testing – III**<br>**Chair: Vishwani Agrawal**, Auburn University<br>**Venue: Room-Dolphin** |
| | **Suchismita R.**, P. Dasgupta and P.P. Chakrabarti, IIT Kharagpur<br>*Bounded Model Checking for Open LTL* | **M.S. Bhat**, Rekha S. and H. S. Jamadagni, CEDT, IISc Bangalore<br>*Multi-level Current-mode Signaling for Long High-Speed Interconnects* | **Sarveswara Tammali** and Jais Abraham, Texas Instruments India<br>*Testing methods, Parameters and Test sequencing for VLSI Devices*<br>**Embedded Tutorial** |
| | **S. Das**, P. Basu, P. Dasgupta and P.P. Chakrabarti, IIT Kharagpur<br>*Syntax-driven Approximate Coverage Analysis for an Assertion Suite against a High-level Fault Model* | **V.B.S. Acharya**, S. Kakde, S. Tantry and Koyama Hiroshi, Sanyo LSI Technology<br>*Design and Implementation of Class AB CMOS Power Amplifier using GSMC 0.15u Technology* | **S.K. Sharma,** Wipro Technologies<br>*Effect of Timing Jitter on High Speed Data Converter System* |
| | K.K. Jha, A. Raychaudhuri, **D. Jain**, Shubha G., David P., Analog Devices and P. Swaroop, NCSU, USA<br>*A 16-bit, 200uA, 10us, Monotonic DAC Converter in SOT-23 package* | Presentation by Participants of the Custom LSI Design Workshop 2005<br>*Lessons Learnt from Custom LSI Design Workshop – Project 1*<br>(**Coordinator: Mahant Shetti**) | **Alok S. Doshi** and V.D. Agrawal, Auburn University, USA<br>*Independence Fault Collapsing* |
| | **S. Chattopadhyay**, IIT Kharagpur, G. Das and H. Bhoumik, SIT Siliguri<br>*Integrated Core and Interconnect Testing with Test-time and Scan Power Minimization* | Presentation by Participants of the Custom LSI Design Workshop 2005<br>*Lessons Learnt from Custom LSI Design Workshop – Project 2*<br>(**Coordinator: Mahant Shetti**) | **T.C.S. Reddy**, M.V. Raghavulu, P. Kalpana, P.T. Vanathi and K. Gunavathi, PSG College of Technology, Coimbatore<br>On-Line BIST for Testing of Operational Amplifiers |
| 3.30 PM - 4.00 PM | Break | | |
| 4.00 PM – 6.00 PM | **Session 4A-5: Panel Discussion**<br>**Need of the Hour for the Indian VLSI Industry – Execution or Innovation?**<br>**Panelists: Mahesh Mehendale**, Texas Instruments, **Raj Khare**, Broadcom, **Rajat Gupta**, Beecem India, **A. Vasudevan**, Wipro<br>**Moderator:** C.P. Ravikumar, Texas Instruments, India<br>**Venue: Room-Coral** | | |
| **End of VDAT 2005 Symposium** | | | |

**Information**

*Please watch updates on VDAT at http://vlsi-india.net The idea behind the VLSI Design And Test (VDAT) Symposium is to promote Research and Development on all aspects of VLSI in India. This symposium is a forum for free discussion of hot and emerging topics in VLSI. It provides a meeting place for VLSI professionals working in India and abroad. We have been holding this event since 1998, and the participation in the event has steadily gone up every year. Until 2004, the event was called "**VLSI Design and Test Workshops**." The VLSI Industry in India and academic community working in the area of VLSI has provided immense support to the symposium.*

*VDAT is sponsored by the **VLSI Society of India**. Please consult http://vlsi-india.net/vsi for more information on VSI"s mission and goals. If you are unable to download the page, please send mail to vsi_india@rediffmail.com for a softcopy of the application form.*
*Consult http://www.vlsi-india.net/vsi/activities/ for updates on the activities of the VLSI Society of India. If you wish to become a member of the VLSI Society of India, you can download the form from http://vlsi-india.net/vsi/membership/. The VSI plans to bring out a journal starting from year 2005. Please wait for announcements.*

# Symposium Committee

**General Chair:**
**C.P. Ravikumar**, Texas Instruments India

## Technical Program Committee

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**Anand Anandkumar**, Magma, India
**P.V. Anandmohan**, ECIL, Bangalore
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**N.S. Murthy**, Philips Semiconductors, India
**D. Nagchoudhuri**, DAIICT, Gujrat, India
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**S. Natarajan**, Emerging Memory Tech., Canada
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**Partha Ray**, National Semiconductor, India
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**R. Varambally**, ST Microelectronics, India
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**Gopal Naidu**, Texas Instruments India

## Website

**Yashdeep Mahajani**, Wipro, India

## Registration Information:

- Registration permits you to participate in all the Technical sessions and Tutorials organized as part of the Symposium, and includes refreshments and lunch on all days.
- Please send your registration fee through a draft made out to "*VLSI Design and Test Symposium, 2005",* payable at Bangalore*.*
- The draft must be sent to *Mr.Gopal Naidu, Finance Chair (VDAT 2005), Texas Instruments India, Bagmane Tech Park, C.V. Raman Nagar, Bangalore 560093.*
- If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Foreign Currency or Credit Card payments.
- The current exchange rate is approximately 1 US dollar = 45 Indian rupees.
- Even those of you who plat to register on the spot are requested to communicate your desire to attend VDAT 2005 to vdat05@hotmail.com with details of vehicle registration number (if any) and laptop number (if any). Without this, you may face difficulties during registration.
- If you are registering for a tutorial, indicate the first and second preference of the tutorial. There are limited seats in each tutorial. If we cannot register you in the tutorial of your choice, we will refund the amount.
- A processing fee of Rs 500/- will be applied against all cancellations.

***Symposium Registration Amount***

| | Fellow | Indian Faculty/ Student | Indian Industry VSI/ IEEE Member | All Foreign Participants | Others |
|---|---|---|---|---|---|
| Before July 15, 2005 | Rs.500/= | Rs.2000/= | Rs.4500/= | US$ 100.00 | Rs.5000/= |
| After July 15, 2005 | Rs.500/= | Rs.2500/= | Rs.5500/= | US$ 150.00 | Rs.6000/= |

***Tutorial Registration Amount***

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|---|---|---|---|---|---|
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| After June 30, 2005 | Rs.500/= | Rs.1500/= | Rs.2500/= | US$ 75.00 | Rs.3000/= |

*Correspondence address for Registration:*
**Mr. Gopal Naidu**
**Texas Instruments (India) Pvt Ltd**
Bagmane Tech Park, Opp. LRDE
C.V.Raman Nagar, Bangalore – 560 093

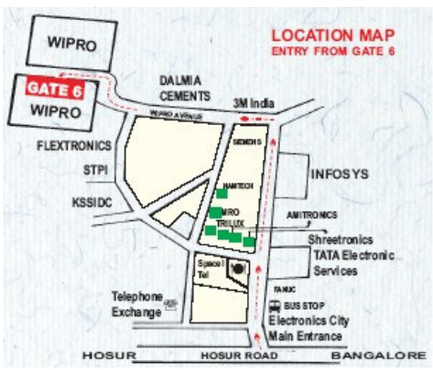
## Venue Information:

The venue of the Symposium is the Learning center on the Wipro campus, located in Electronics City. Each of the rooms has a capacity of 100. All Rooms have video hooking for the plenary events. Speakers will have facilities such as DLP projector, cordless microphone, and whiteboard.

Since the conference venue is on Wipro Campus, we need to work with the Security personnel of the organization to make the process of registration a smooth one. Your cooperation in this regard is appreciated. Please send mail to vdat05@hotmail.com and inform your vehicle's registration number and Laptop number if you will come in your private vehicle and/or bring your laptop.

There are several hotels in Bangalore and information on these is available from the Internet. We plan to provide bus pickup/drop service from the following two areas: (a) Indian Institute of Science (b) Majestic. Details will be announced on the website. If you plan to use your own transport, please note: to reach Electronics city, you must travel on Hosur road and enter the Phase I gate. See the location map shown here. The distance to the venue from Railway station is ~20 km and from the Airport, about 15 km**.** Due to traffic during morning rush hour and evening rush hour, the actual transit time may be significantly high. ***Please plan your travel***.

Weather in Bangalore during August is pleasant, bordering on chilly, with occasional showers.




## History of VDAT:

| Event Title | Venue | Date | Participants |
|---|---|---|---|
| 1st VDAT | Chennai | January 7, 1998 | 30 |
| 2nd VDAT | New Delhi | August 6-7, 1998 | 70 |
| 3rd VDAT | New Delhi | August 20-21, 1999 | 120 |
| 4th VDAT | New Delhi | August 25-26, 2000 | 150 |
| 5th VDAT | Bangalore | August 16-18, 2001 | 220 |
| 6th VDAT | Bangalore | August 29-31, 2002 | 300 |
| 7th VDAT | Bangalore | August 28-30, 2003 | 300 |
| 8th VDAT | Mysore | August 26-28, 2004 | 250 |

VLSI Society of India

# 9th IEEE VLSI Design & Test *Symposium*

**August 10-13, 2005**

**Venue:** Learning Center, Wipro Campus, Electronics City, Bangalore, India

## Registration Form:

| | |
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| 1. Name of the participant: | |
| 2. Affiliation | |
| 3. Permanent Mailing address: | |
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| | |
| 4. E-mail Address (mandatory): | |
| 5. Telephone: | |
| 6. If you are not part of the VDAT e-mail list, would you like to be included? | **Yes** ☐ / **No** ☐ |
| 7. If you plan to come by your own vehicle, indicate your Vehicle number | |
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*You can also download this form from the VDAT Website:*
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***Tutorial Registration Amount***

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| Before June 30, 2005 | Rs.500/= | Rs.1000/= | Rs.2000/= | US$ 50.00 | Rs.2500/= |
| After June 30, 2005 | Rs.500/= | Rs.1500/= | Rs.2500/= | US$ 75.00 | Rs.3000/= |

*Make the Draft payable at Bangalore, to "***VLSI Design & Test Symposium 2005***"*

| | | |
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| **Total Amount:** | **DD No.:** | **Dated:** |

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