## **VLSI Design and Test Symposium**

August 10-13, 2005 Bangalore, Karnataka

http://vlsi-india.net

# **Intent to Participate**

- 1. Name of the participant:
- Affiliation
- Permanent Mailing Address:
- Email Address:
- 5. FAX Number:
- Telephone Number:
- 7. Do you wish to submit a paper to VDAT 2005? (Yes/No)
- 8. Have you applied for a fellowship to attend VDAT 2005? (Yes/No)
- 9. If you are not part of the VDAT e-mail list, would you like to be included? (Yes/No)

You can download this form from the VDAT Website:

http://vlsi-india.net

After completing this form, please mail it to:

Mr. Gopal Naidu

Texas Instruments (India) Pvt Ltd Bagmane Tech Park, Opp. LRDE

C.V.Raman Nagar, Bangalore - 560 093 vdat05-regn@hotmail.com

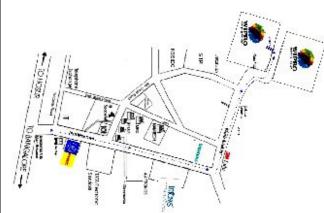


# About Bangalore:

Bangalore is the *silicon valley* of India and houses hundreds of companies working in all aspects of VLSI and embedded systems. Bangalore is also known as the Garden City of India. The venue of the Symposium is the "floating" learning center on the Wipro campus, located in Electronics City.

There are several hotels in Bangalore and information on these is available from the Internet. To reach Electronics city, you must travel on Hosur road and enter the Phase I gate. The distance from Railway station is ~20 km and from the Airport, the distance is ~15 km.

The weather in Bangalore during August will be pleasant, with occasional showers.



**Location Plan: Entry from Gate-6** Updated 23-Jan-05



## CALL FOR PARTICIPATION 9<sup>th</sup> IEEE VLSI Design & Test

**Symposium** August 10-13, 2005 Bangalore, India

Sponsored by



VLSI Society of India Industry Sponsors: Wipro, TI India

In Cooperation With:



IEEE-CS-TTTC and IEEE EDS/SSCS Bangalore Chapter IEEE CAS Bangalore Chapter (Confirmation Awaited) http://vlsi-india.net

Related Site - http://vlsi.nj.nec.com/

# **Tracks in VDAT Symposium:**

Track on High-level Design will discuss issues related to system-level synthesis, microarchitecture, embedded systems, codesign, core-based design of SoC, timing convergence, high-level synthesis, logic synthesis, memory synthesis, and FPGA synthesis. Track on Physical Design and VLSI Technology will discuss all issues related to physical design and process related aspects of integrated circuits, such as layout, fabrication, packaging, optoelectronic circuits, MEMS, deep submicron and nanometer devices. Track on Testing and Verification will discuss issues related to testing, testability, and verification of digital designs, memories, analog designs, and mixed-signal designs, and circuits containing deep-submicron and nanometer devices. Full-day Tutorials will be held on August 10, 2005.

**Venue** – The tutorials and the symposium will be held at the Learning Center, Wipro Campus, Electronics City.

### **Conference Committee**

#### General Chair:

C.P. Ravikumar, Texas Instruments India

#### **Technical Program Committee**

Program Committee
Vishwani Agrawal, Auburn University, USA
Anand Anandkumar, Magma, India
P.V. Anandmohan, ECIL, Bangalore
Shabbir Batterywala, Synopsys, India
Navakanta Bhat, IISC, Bangalore, India
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S. Natarajan, Emerging Memory Tech., Canada

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C.P. Ravikumar, Texas Instruments, India

Partha Ray, National Semiconductor, India

J.N. Roy, Punjab University, India

Vineet Sahula, MREC Jaipur

Dinesh Sharma, IIT Bombay, India

Alok Singh, Virage Logic, India

S. Srinivasan, IIT Madras, India

R. Varambally, ST Microelectronics, India

G. Vidyasagar, Texas Instruments India

V. Visvanathan, Texas Instruments, India

### **Local Organization Chair**

C.R. Venugopal, SJCE, Mysore

### **Finance Chair**

Gopal Naidu, Texas Instruments India

#### Website

Yashdeep Mahajani, Wipro

#### **Organizing Committee**

Navakanta Bhat, Indian Institute of Science Vishal Dalal, Sasken Rajesh Babu Vasu, Wipro Anuj Sharma, Wipro Harindranath M. Nair, Wipro Amitabh Ojha, Wipro C.P. Ravikumar, Texas Instruments, India

#### **Fellowships Chair**

Dr Narasimha Kaulgud, Wipro (vdat05-fellow@vlsi-india.net)

### ADDRESS FOR CORRESPONDENCE

Authors should submit full papers of **at most 10 A4-size pages, including figures and references**. Submissions will undergo blind review – the authors must not include their names or affiliations in the submissions. Your submission should represent original contribution and should not have been submitted to other forums. It is important that abstracts bring out the contribution and novelty of the paper. *Survey papers are not acceptable as submissions*. However, proposals for embedded tutorials (1 hour or 2 hour duration), full-day and half-day tutorials, and proposals for panel discussions are invited. Please indicate clearly in the submission that your submission is a proposal for an embedded tutorial. Send your submissions through the Docman system accessible from <a href="http://vlsi-india.net">http://vlsi-india.net</a> as well as <a href="http://vlsi-india

For questions relating to technical program, submissions, and sponsorships, write to:

C.P. Ravikumar

Texas Instruments, India Bagmane Tech Park, CV Raman Nagar, Bangalore 560093

Email: ravikumar@vlsi-india.net

FAX: 91-80-25048213

Submitting authors must become members of the <a href="vdat@yahoogroups.com">vdat@yahoogroups.com</a> mailing list, where updates on the symposium will be sent.

### IMPORTANT DATES

Last Date for paper submission: March 15, 2005 Last Date for Tutorial submission: March 31, 2005 Notification of acceptance: May 1, 2005 Last day to receive final manuscript: June 1, 2005

Symposium Dates: August 11-13, 2005

## Sponsorships:

A company can sponsor VDAT by making a payment of Rs. 1,00,000/=. The sponsorship money will be used to support fellowships.

## Fellowships:

If you are a postgraduate student from India specializing in VLSI or a faculty member from India with interest in VLSI, you can apply for a full or partial fellowship. If you are an undergraduate student who has submitted a paper to VDAT, you are eligible for a fellowship. Fellowship includes one or all of the following: registration fee waiver, travel reimbursement and accommodation. Use the Fellowship format given adjacent.

# History:

<b>Event Title</b>	Venue	Date	Participants
1st VDAT	Chennai	January 7, 1998	30
2 <sup>nd</sup> VDAT	New Delhi	August 6-7, 1998	70
3rd VDAT	New Delhi	August 20-21, 1999	120
4th VDAT	New Delhi	August 25-26, 2000	150
5 <sup>th</sup> VDAT	Bangalore	August 16-18, 2001	220
6 <sup>th</sup> VDAT	Bangalore	August 29-31, 2002	300
7 <sup>th</sup> VDAT	Bangalore	August 28-30, 2003	300
8th VDAT	Mysore	August 26-28, 2004	250

## Fellowship Form:

- 1. Name:
- 2. Institution and Departmental Address:
- 3. Status: Student/Faculty (You should be a faculty or a student at the time of the Symposium to avail fellowships):
- 4. Email Address (mandatory):
- 5. Contact Address:
- 6. Experience in VLSI Field: (Teaching/ Projects):
- 7. Can your parent Institute support you partially? If not, please include a letter from your Head or Principal to that effect and recommending your name for a fellowship.
- 8. Have you submitted a paper to VDAT 2005?
- 9. Have you received Fellowship to attend VDAT before?
- 10. Do you need accommodation at Bangalore?
- 11. Attach your brief Bio-data along with this form. Please have your application forwarded by your HOD or Principal or your Institute. Send the form to reach the Fellowships Chair through e-mail by **May 15, 2005**. If you are granted fellowship, you are expected to attend the event on all days.