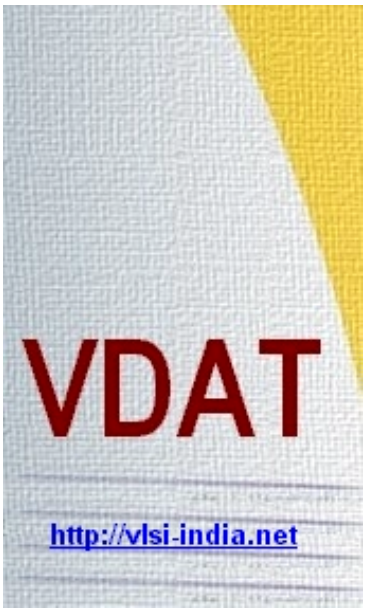

VLSI Design and Test Workshops 2003

Advance Program

(Latest version available at http://vlsi-india.net)

August 28-30, 2003

Bangalore, India

Scope: To promote applications and research related to all aspects of VLSI

In Cooperation With: *VLSI Society of India, IEEE Computer Society Technical Council on Test Technology IEEE EDS/SSCS Bangalore Chapter*

With Support From: *Texas Instruments, India, Indian Institute of Science.*

Venue: **JN Tata Auditorium, Indian Institute of Science, Bangalore**

For The Latest Registration Information:

http://vlsi-india.net/latest/registration.html

http://members.tripod.com/vlsi_india/latest/registration.html

Advance program for August 28, 2003 (VLSI Education Day)

8.00 to 9.00 AM	**Registration**	
9.00 to 9.15 AM	**Inauguration**	
9.15 to 10.15 AM	**Keynote Talk:** **Chandra Shekhar**, IC Design Group CEERI, Pilani *VLSI Education in India: Towards Excellence, Numbers, and Relevance*	
10.15 to 10:45 AM	**Tea Break**	
	Session E3: Student Projects in VLSI: Setting up for Success **Chair: TBA** **Moderator: C.P. Ravikumar** **"Speakers include M. Balakrishnan** *IIT Delhi* **and H.S. Jamadagni** *IISc, Bangalore*.**"**	
10.45 AM -- 12.15 PM	*Students and faculty face several challenges in executing successful projects in VLSI area. While projects in IT areas such as networking require much less infrastructure, the same is not the case for VLSI design projects. Moore's law has the potential to outdate equipment in a short span of time. Standards are continuously changing or evolving. How can students and faculty deal with these problems? Will industry-academia interaction provide some solutions? How can these relations be sustained? Invited speakers will discuss the problems faced in executing VLSI projects and suggest solutions.*	
	Session E4: Tutorial on MEMS **Chair: Chandra Shekhar**	**Session E5: Tutorial on Reliability** **Chair: Venugopal Puvvada**
12.15 to 1.15 PM	**N. Bhat,** C. Venkatesh, and S. Patil, Indian Insittute of Science. *Micro Electro Mechanical Systems (MEMS): An Overview.*	**M.K. Radhakrishnan,** Philips, Singapore. *Deep Sub-Micron CMOS: Reliability Issues Related to Design and Process*.

1.15 to 2.15 PM	**Lunch and Time to Visit Exhibits**

2.15 to 3.45 PM	**Session E6:** **Frequently Not Asked Questions!** **Moderator: C.P. Ravikumar**, **Panelists: Shabbir Batterywala, Rubin Parekhji, M. Balakrishnan, Navakanta Bhat** *Experts from industry and academia will answer technical questions posed by engineers and students on various aspects of VLSI Design/CAD. Questions may be sent to cpravikumar@rediffmail.com*

3.45 PM – 4.15 PM	Tea

4.15 to 5.45 PM	**Session E7: Teaching VLSI: Blue Skies and Pot Holes** **Moderator: C.P. Ravikumar** **Panelists**: **M. Balakrishnan** *IIT Delhi*, **H.S. Ramakrishna** *Brandcom,* **Vishwani Agrawal** *Rutgers University*, **Ashok Rao** *IISc* *A large number of VLSI design/EDA companies, including several multinationals, have been established in India over the past decade. This has motivated several academic institutions to start postgraduate programs in VLSI. What are the challenges in starting and sustaining these programs? What needs to be done to sustain the quality of VLSI education?*

5.45 to 6.00 PM	Snack Break

	Session E8: Poster Papers I **Session Chair: S. Bose**	**Session E9: Poster Papers II** **Session Chair: V. Sahula**
6.00 to 7.00 PM	**(P) H. Thapliyal and V. Verma,** GB Pant University. *A High Speed Efficient Signed/ Unsigned NxN Bit Multiplier Based on Ancient Indian Vedic Mathematics.*	**D. Jain,** BITS Pilani; S.C. Bose, CEERI Pilani; S.N. Sharan, GCET, Noida. *Performance Analysis of FPGA.*
	(P) A. K. Gupta and N. Bhat, Indian Institute of Science. *A Low Power Circuit to Generate Neuron Activation Function and its Derivative using Back Gate Effect.*	**Ramachandran B**; V. Vishwanath P.L. *Design, Synthesis and Implementation of an RBF Neural Network based Multi-user Detector for MC-CDMA System in FPGA.*
	(P) B. Bala Tripura Sundari; K. Murali Krishna, Amrita Institute of Technology, Tamil Nadu. *HDL Implementation of Deterministic Traffic Regulator.*	**A. Garimella**, MAHE, Manipal. *Full Custom VLSI Implementation of Golay and Extended Golay Encoder and Decoder.*
	(P) N.J.R. Muniraj, R.S.D.Wahida Banu, N.Prabhakaran, P.Antony Vimal Dass, Sona College of Technology, Salem. *Implementation of Blind Adaptive Filtering- Using VLSI Technology.*	B. Sharma**; S. Dasgupta**, Indian School of Mines, Dhanbad. *Application of Non-Equilibrium Green's Function Formalism for Nanometric MOS Device Modelling and Simulation.*
	(P) K. Paramasivam, Amrita Institute Of Technology, Coimbatore; K. Gunavathi, PSG College of Technology, Coimbatore. *VLSI Design Simulation for Routing in Communication Network using Parallel Architecture.*	**(P) S. Joseph,** Christ College, Bangalore. *Discussion, Comparison and Hardware Implementation of DCT Algorithms for Image Processing.*

Exhibits
Book Exhibit by In-Touch and University Booth will be located in the foyer area of JN Tata Auditorium during 9.00 AM -6.00 PM.

Advance Program for August 29, 2003 (Friday)

Time	**Test Workshop** **Room: A**	**High Level and Logic Design Workshop** **Room: B**	**Physical Design and VLSI Technology Workshop** **Room: C**
8:00 to 9:00 AM	***Registration***		
9.00 to 10.00 AM	**Session L1 : Keynote Talk I** **Chair: Nagaraj Subramanyam** **R. Camposano, Synopsys, USA**. *The Growing Semiconductor Zoo: ASICs, Structured Arrays, FPGA, Processor Arrays, Platforms and other Animalia*.		
10.00 – 10.30 AM	***Tea Break***		
	Session T1: Test & Verification I **Chair: Vishwani Agrawal**	**Session L2: Design Techniques** **Chair: S. Mahant-Shetti**	**Session P1: Devices and Technology** **Chair: D. Nagchoudhuri**
	(R) R.K. Dasari; Krishna Kumar D, Mentor Graphics, India. *Framework for verifying Assertions using sequential ATPG.*	**(R) D. Chakrobarty**, M.B. Srividya, A. Bhattad, S. Mahant-Shetti, *KARMIC. CMOS Camera with Electronic Shutter*.	**M.K. Radhakrishnan**, Philips, Singapore. *ESD in Sub-Micron Devices: Issues and Challenges.*
	(R) P.K. Dakhole. *Coverage-Driven Functional Verification: Coverage to Speed Verification and Ensure Completeness.*	**(R) L.V.Holla**, P.Vallur, P.T.Balsara, A.Navada, S.Shastry, University of Texas, Dallas. *A Fast 16-bit TSPC Adder in SOI CMOS*	**(R) J.N. Roy**, SCL Chandigarh. *Optimized Output Structure For Visible Imager Charge Couple Devices*. *Invited Talk.*
	(S) N.K. Soni; **S. Chattopadhyay,** IIT Guwahati. *Test Data Compression for System-on-Chip using an Adaptive Code.*	**(S) V.Jindal**; Alpana Agarwal. *Carry circuitry for LUT-based FPGA (optimized for implementing finite field multipliers)*	**(S)** V.K. Gupta; **S. Dasgupta**, Indian School of Mines, Dhanbad, India. *Modelling and Simulation of Quantum Dot Cellular Automata (QCA) for Future Nanometric Devices.*
	(S) **H. Rahman**; D. K. Das; Bhargab B. Bhattacharya, ISI Calcutta. *Universal Test Set for Detection of Stuck-at-Faults in GRM (Generalized Reed-Muller) Circuits.*	**(S)** Indu S, CRL, Bharat Electronics Ltd.**; Avinash K.R**, Wipro Technologies, Bangalore. *VLSI Implementations of Image Resizing Algorithms Issues and Proposed Solutions.*	**(S) D.K.Maurya**; K.Biswas; S.Das & S.Kal, IIT Kharagpur. *Fabrication of Silicon Membrane at the Free End of Cantiliver by Wet Anisotropic Etching.*
	(S) K. Katiyar, Texas Instruments India. *Dual Processor Model based Verification of SoC.*		**(S) P.Chakrabarti**; S Nayak; D. Mishra; N. Jain, Banaras Hindu University. *A Proposed Laser Pre-Amplified Optoelectronic Integrated Circuit (OEIC) Receiver Based on a Single MESFET Front-End.*
12.30 to 2.00PM	***Lunch***		
2:00 to 3.00 PM	**Session L3: Keynote Talk II** **Speaker: Vasudevan Aghoramoorthy**, *Wipro Technologies* *Semiconductor Design Outsourcing: Global trends and Indian Perspective* **Chair: TBA**		
3:00 to 3.30 PM	***Tea Break***		

	Session T2: Test and Verification II **Chair: R. Parekhji**		**Session L4: EDA I** **Chair: C.P. Ravikumar**

3.30 – 5.30 PM	**(R) V. D. Agrawal**, Rutgers University; A.V.S.S. Prasad**,** M. V. Atre, Agere Systems, Bangalore. *It is sufficient to test 25-Percent of Faults.*		**(R) A. Mehrotra**, L. van Ginnekan; Y. Trivedi, Magma Design Automation, USA. *Design Flow and Methodology for 50M Gate ASIC.*
	(R) J. Abraham, Texas Instruments India**.** *Test Cost Computation and Reduction Techniques.*		**(S)** P. Cavale; **A. Pandey**; Krupakaran A., Spike Technologies, Bangalore, India. *Seamless Physical Design Flow- Challenges and Solutions.*
	(S) Asha B.P., CG CoreEl, Bangalore, India. *Reduced Pin Count Testing Using IEEE 1149.1 Environment.*		**(S)** Suresh Krishnappa; **S. Chattopadhyay,** IIT Guwahati. *Partitioning of Circuits for Mapping onto Dynamically Reconfigurable FPGAs.*
	(S) S.S. Singh and **S. Chattopadhyay**, IIT Guwahati. *Genetic Algorithmic Technique for Integrated Testing of Cores and Interconnects in SoCs*		**(S) R. Bhooshan**; V. Rakhecha; B. Abraham; V.Singhal; V.Puvvada. Texas Instruments India. *A Unique Method for Dynamic Voltage Drop Analysis and Decoupling Capacitance Estimation*.
	(S) A.Gangwar, R.K. Dasari, Shiva Kumar K, Mentor Graphics, Hyderabad, India. *A Study of Parallel Test Application for Core Based SoC Designs.*		**(S) A. Bidve**; P. Rohilla, ST Microelectronics, Noida, India. *Useful Skew Management Inside Standard Cell Library.*
5.30 to 6.00 PM	*Snack Break*		

	Session L5: Poster Papers I **Chair: Debesh Das**	**Session P2: Poster Papers II** **Chair: D. Nagchoudhuri**
6.00 to 7.00 PM	**(P) C. M. Umapathy,** CelStream Technologies Private Limited, Bangalore. *Low Power Area Efficient Digital Counters.*	**(P) R.K. Pal,** University of Calcutta. *Channel Sort: A Sorting Algorithm by Constructing Instances of Channel Routing Problem*
	(P) Govind S.; S. Choudhury; V. Sahula, MNIT, Jaipur. *Optimizing ARM7 like Processor Architecture for Video Applications (Motion Estimation).*	**(P) S. R. Reddy,** Indira Gandhi Institute of Technology, GGSIP University, Delhi. *GUI for Embedded Systems Design.*
	(P) K. Bharath; M. Mani. *A Wide Range, High Linearity VCO.*	**(P)** P. Chakravorty, D. Chakraborty, **S. Bose**, Calcutta University**.** *A Simple Rectilinear Steiner Tree Algorithm for VLSI Global Routing.*
	(P) N. Bhatia, Tejas Networks. *Design Challenges: Virtual Concatenation, Next Generation Sonet/ SDH*	**(P) H. Mangalam,** Sri Krishna College of Engg. & Technology, Coimbatore; K. Gunavathi, PSG College of Technology, Coimbatore. *Power Optimal Clock Distribution in VLSI Circuits.*
	End of Day 1	

Advance Program for August 30, 2003 (Saturday)

Time	**Test Workshop** **Room: A**	**High-level and Logic Design Workshop** **Room: Main Auditorium**	**Physical Design and VLSI Technology Workshop** **Room: B**
9.00 – 10.00 AM	**Session L6: Keynote Talk III** **Chair: TBA** **Mahesh Mehendale**, Texas Instruments India. *Concurrent Engineering – Challenges and Opportunities.*		

10.00 – 10.30 AM	*Tea Break*		
	Session T3 Test Generation **Chair: Anand Moghe, Mentor Graphics**	**Session L7: Low Power Design** **Chair: V. Visvanathan**	**Session P3: Physical Design I** **Chair: Dinesh Sharma**
11.00 – 11.30 AM	**K. Shiva Kumar**, Mentor Graphics, Hyderabad. *Embedded Test for SoC Design. Tutorial.*	**P.R. Panda**, IIT Delhi. *The Energy Impact of Memory Port Allocation Decisions. Invited Talk.*	**(R) S. Deb**; N. Bhat, Indian Institute of Science, Bangalore, India. *Design and Implementation of Passive RF Tag IC.* **(R) V. Narang**; K. Rajgopal, Texas Instruments India. *Architectures for Noise Rejection in Level Shifting CMOS Receivers.*
11.30 AM – 12.00 PM	**(S) A. Oke**; Srinivas Kumar Vooka; R. A. Parekhji, Texas Instruments India. *Estimating Fault Coverage of SoCs Using Module Coverage Data.*	**(R)** P. Rajeshwari**; V. L. Prabha,** Government College of Technology, Coimbatore; E. Chandra Monie, TPGIT, Vellore. *Power Management in Embedded Systems by an Efficient Online Idletime Prediction Scheme.*	**(S) A.S. Mandal,** CEERI Pilani**;** B. Bhaumik, IIT Delhi. *Techniques for Improving the Neural Optimization Method.*
12.00 – 12.30 PM	**(R) A. Kokrady,** Texas Instruments India; R. Mehrotra, NSIT, New Delhi; C.P. Ravikumar, S. Phani Kumar, Texas Instruments India. *Estimating Power Dissipation of Embedded Memories***.** **(S)** D.Jain, BITS Pilani; **S.C. Bose,** Chandra Shekhar, CEERI Pilani. *Detection and Analysis of Faults of CMOS OP Amp*	**(R) S.S. Abrar**, Philips, India. *Novel Source- Independent Characterization Methodology for Embedded Software Energy Estimation.*	**(S) B. Choudhury**, ST Microelectronics, Noida, India. *Design for Manufacturability in Analog and Digital Library Development for High Semiconductor Reliability.* **(S) C. S. Thakur**; N. Bhat, Indian Institute of Science, Bangalore, India. *Impact of Gate to Source/ Drain Overlap for Analog CMOS Circuit Application in sub-100nm Technology.*
12:30 to 1:30 PM	*Lunch*		
	Session L8: EDA II **Chair: P.R. Panda** **Venue: Room B**		**Session P4**: **Physical Design II** **Chair: Navakanta Bhat** **(Venue: Main Auditorium)**
1:30 to 1.50 PM	**(S) S. Chakraverty,** NSIT, New Delhi, India**.** *An Availability Model for Cosynthesis of Real-time System.*		**(R) D. Sharma,** L. Kumath, A. Gupta, IIT Mumbai. *High Speed Sigma-Delta Modulators. Invited Talk.*
1.50 to 2.20 PM	**(R) T.S. Rajesh Kumar,** C.P. Ravikumar, R. Govindarajan. *Memory Architectures for Multiprocessor Embedded Systems.*		**(R)** A. Mandal; S. Ramanathan; S. Shrivastava; **S. Chandrasekar**, Texas Instruments India. *Crosstalk Noise Closure in DSM Designs.*
2.20 to 2.40 PM	**(S) M. Desai**, DAIICT, Gujarat, India.*Re-configuration in SoC Using Programmable Interconnect.*		**(S) A. Pandey**, ST Microelectronics; B. Bhaumik**,** IIT Delhi**.** *Automation of Analog Layout Generation and Design: Parameterized Cell Library Approach.*
2.40 to 3.00 PM	**(S)** A.G. Somayaji; **G. Thareja**; G. Kapila; V. Rakhecha, Texas Instruments India. *Static Approach for Peak Power Supply Noise Estimation.*		
3:00 to	*Tea*		

3:30 PM	
4.00 to 6.00 PM	**Session L9 Panel Discussion** **Moore's Law: At what cost?** *Has Moore's law reached a point of diminishing returns? What is the impact of the IT recession on VLSI industry? How do we shape the future? How should India position itself at this turning point? These are some of the questions that the panelists will debate.* **Coordinator: C.P. Ravikumar** **Panelists: Mahesh Mehendale** *Texas Instruments, India*, **Mahesh Rao** *Aspirenet Communications*, **Sandeep Relan** *Broadcom*, **Dinesh Sharma** IIT Bombay

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Registration Information:
Registration permits you to participate in all the technical sessions and tutorials organized as part of the workshops. Refreshments and lunch will be provided to all registrants at no extra charge. Please send your registration fee through a draft made out to *VLSI Design and Test Workshops, 2003*. ***Make the draft payable at Canara Bank, IISc, Bangalore Branch.*** The draft must be sent to **Prof. Navakant Bhat, Department of Electronics and Communication Engineering, Indian Institute of Science, Bangalore, 560 012**, India. If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Foreign Currency or Credit Card payments. The current exchange rate is approximately 1 US dollar = 45 Indian rupees.

Registration Fees Before July 28, 2003

	Indian Participant	Foreign Participant
Academic Institution	Rs. 2000	USD. 50

Non-academic Institution	Rs. 5000	USD. 150

Registration Fees After July 28, 2003

	Indian Participant	Foreign Participant
Academic Institution	Rs. 2500	USD. 75
Non-academic Institution	Rs. 6000	USD. 175

Venue Information: The JN Tata Auditorium is located in the National Science Seminar Complex of the Indian Institute of Science, popularly known as the "Tata Institute." The institute is located close to Yashavantapuram and Malleshwaram. If you are going to take a Taxi or an Autorickshaw, ask the driver to take you to the *Tata Institute*. There is a separate gate to enter the JN Tata Auditorium.

- More information about the Indian Institute of Science is available from http://iisc.ernet.in.
- A map of IISc is available from http://cm.bell-labs.com/cm/cs/who/va/(Look for Conference Site)
- Some useful websites which provide information on hotels and tourism in Bangalore are: http://www.geocities.com/Athens/2960/www.bangalorehotels.net/http://www.virtualbangalore.com/Tou/index.php3

Weather Information: The weather in Bangalore during August is pleasant (temperatures ranging in 25 degrees to 30 degrees centigrade), with intermittent rain.

Fellowships: A small number of full or partial waivers of registration fee are available for Indian post-graduate students and Indian faculty. Fill out an application form at http://vlsi-india.net and send a hard copy of the same duly attested by your Head of the Department with a statement of purpose for attending the workshops before July 1, 2003 to ***Prof. Harishchandra Hebbar, Fellowships Chair, VDAT 2003, MCIS, Manipal Academy of Higher Education, Madhav Nagar, Manipal*** - *576119.* A limited number of rooms in hostels and guesthouses at the Indian Institute of Science are available for fellows. Mr G.C. Deepak (gcdeepak@ece.iisc.ernet.in) will keep the fellows informed about accommodation.

Related Event: International Conference on VLSI Design, New Delhi, 2003: http://vlsi.ccrl.nj.nec.com/