VLSI chips on three-dimensional closed surfaces

Satrajit Ghose[1], *Susmita Sur-Kolay*[2], *Bhargab B. Bhattacharya*[1]

Keywords : Three-dimensional VLSI, routing.

ABSTRACT

The evolution of VLSI fabrication technology over the last two decades has resulted in complex chips as well as MCMs (multi-chip modules) with very high computational capabilities. However, the associated increase in the number of interconnections has been reflected on the increase in the number of metal layers from two to several dozen in MCMs. Currently, MCMs still have one layer of active devices, usually the top-most starting from substrate upwards. Routing plays a critical role in VLSI system design as it strongly influences the system performance in terms of timing, power and paricularly, the interconnection area which dominates the layout area.

Fabrication of three-dimensional ICs having more than one active device layer (all-active volume) were carried out more than a decade ago [1]. Case studies of layout costs [3, 4] in three-dimensional VLSI with either all-active volume or one-active volume were reported. The present day MCM falls into the one-active category. Routing algorithms for three-dimensional chip which have only one active layer as in MCM, were designed in [2].

In this paper, we propose a novel three dimensional layout scheme with one-active volume for VLSI/MCM chips with the goal of reducing routing costs considerably. This scheme looks ahead of the current state-of-the-art deep submicron technology which will soon reach the limits of semiconductor device physics.

The average rectilinear routing cost between two randomly chosen points on a plane rectangular surface diminishes if we join any two of its parallel edges. This idea is elaborated to propose a three dimensional routing model for MCMs in which the layout surface is a closed one. We say that a surface is routing efficient if the average cost of routing on it is about 20% less than that for routing on a plane rectangle of same area.

The chips are placed on the outermost layer of closed surface. To perform successsful routing, concentric inner layers are added as required. To search for a simple and efficient surface, a theorem to evaluate average rectilinear distance of two randomly chosen points in N dimensional orthogonal space for inside routing, is used to calculate the routing cost reduction for different 3D surfaces. For given surface area, the average recilinear distance is reduced by
(i) 33.31% for routing on the faces of a cube;
(ii) 25% for routing on a cube except the top and bottom faces;

[1]Advanced Computing & Microelectronics Unit, Indian Statistical Institute, Calcutta 700035, India. e-mail: {res9706,bhargab}@isical.ac.in

[2]Dept. of Computer Science and Engg., Jadavpur University, Calcutta 700032, India. e-mail: elcv9602@isical.ac.in

(iii) 29.3% for routing on a rectangular parallelopiped with square base of perimater twice the height but not on top or bottom face.
(iv) For a right circular cone, the optimum reduction of 42.26% occurs when its circumference is 6 times the slant height.
(v) For a sphere the reduction turns out to be 35.18%. By adding concentric layers for routing, the cost reduction is expected to be higher.

The search for an efficient and easily implementable surface ends with rectangular tube for which the volume of occupancy is 70.7% of a cube shaped tube. The core of the concentric tubes can be a silicon ingot. The external I/O pins are placed on a designated surface. Thermal constraints may be tackled by having a hollow core. The fabrication issues have to be analysed in detail.

Software simulation for successful routing is under progress and the experimental results are expected to support the theoretical insight. This futuristic scheme also opens up a range of open problems related to floorplanning/placement.

References

[1] Y. Akasaka, "Three-dimensional IC trends," Proc. of the IEEE, 74(12): 1703-1714, 1986.

[2] C. C. Tong and C. Wu, " Routing in a three-dimensional chip," IEEE Trans. on Computers, 44(1): 106-117, 1995.

[3] F. P. Preparata, "Optimal three-dimensioal VLSI layouts," Mathematical System Theory, 16: 1-8, 1983.

[4] A. L. Rosenberg, "Three-dimensional VLSI: A case study," J. ACM, 30(3): 397-416, 1983.

[5] N. A. Sherwani, S. Bhingarde and A. Panyam, *Routing in the Third Dimension*, IEEE Press, 1995.