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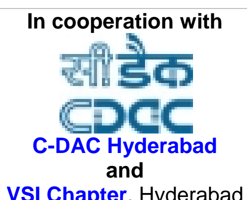
VLSI Society of India

Short Course on Digital Circuits Test and Design For Test

August 11-14, 2008, Hyderabad, India
Venue: Hotel Green Park
Greenlands, Begumpet, Hyderabad, Tel : 091 - 040 - 66515151, 23757575
Green Park - Hyderabad

In cooperation with



C-DAC Hyderabad
and
VSI Chapter, Hyderabad

Past courses
DCT-DFT 2006
Aug 17-19
Bangalore
DCT-DFT 2007
Aug 13-17
Noida, UP

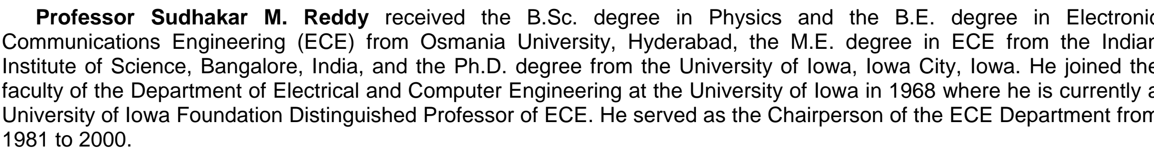
Summary:

Testing of every manufactured device is necessary to ensure product quality. As the complexity of electronic integrated circuits grows, their testing has also become very complex and expensive. This course will provide an overview of the recent trends in testing of digital circuits and designing these circuits for better testability.

Targeted Audience:

Targeted audience is practicing engineers, students and academics.

Course conducted by: **Prof. Sudhakar M. Reddy**, Iowa University; **Dr. Nilanjan Mukherjee**, Mentor Graphics Corporation, US; and **Dr. C.P. Ravikumar**, Texas Instruments India



Professor Sudhakar M. Reddy received the B.Sc. degree in Physics and the B.E. degree in Electronic Communications Engineering (ECE) from Osmania University, Hyderabad, the M.E. degree in ECE from the Indian Institute of Science, Bangalore, India, and the Ph.D. degree from the University of Iowa, Iowa City, Iowa. He joined the faculty of the Department of Electrical and Computer Engineering at the University of Iowa in 1968 where he is currently a University of Iowa Foundation Distinguished Professor of ECE. He served as the Chairperson of the ECE Department from 1981 to 2000.

Professor Reddy has published well over four hundred papers in archival journals and the proceedings of international conferences. Several papers co-authored by him received best paper nominations and awards. Professor Reddy has given keynote talks at international conferences. He has also given one-day tutorials to practicing engineers at international conferences. He received a Von Humboldt Prize in 1995 and the first Life Time Achievement Award from the International Conference on VLSI Design. Professor Reddy is a Life Fellow of IEEE.

Professor Reddy has served on the committees of several international conferences. He was the Technical Program Committee Chair of the 1989 Fault Tolerant Computing Symposium. He has served twice as a guest editor for the special issues on Fault Tolerant Computing and as an associate editor of the IEEE Transactions on Computers and has been serving as an associate editor of the IEEE Transactions on CAD for the last ten years.

Nilanjan Mukherjee received a B.Tech.(Hons) degree in Electronics and Electrical Communications Engineering from IIT Kharagpur, India, and a Ph.D. degree in Computer Engineering from McGill University, Montreal, Canada. He has been with Mentor Graphics since 1999 and is currently Director of Engineering for the Test Synthesis Group in the DFT division. He is a co-inventor of the Embedded Deterministic Test Technology and was a lead developer for TestKompress, the leading test compression tool in the industry. Prior to Mentor, he was with Bell Laboratories at Lucent Technologies.

Nilanjan has published over 45 technical papers at various international conferences and refereed journals. He is a co-author of the paper on "Embedded Deterministic Test" in IEEE Transactions on CAD that won the Donald O. Pederson award in 2006. In addition, his paper on the same topic at ITC 2002 has been recognized as one of the most significant papers in the past 35 years of ITC. He received the Best Paper Award at the VLSI Test Symposium in 1995 and co-authored a paper that received the Best Student Paper award at the 2001 Asian Test Symposium. Nilanjan is a co-inventor of 14 US patents.

Nilanjan has presented numerous tutorials and seminars at major conferences like ITC, DAC, and VLSI Design, as well as at various Mentor Graphics events in US and India. He was the General Chair for the 2008 International Test Synthesis Workshop and has been in the Program Committee of numerous conferences such as ITSW, VLSI Design, ATS, DDECS, and VDAT.

Dr. C.P. Ravikumar is with Texas Instruments India as a Senior Technologist in VLSI Test. Before joining TI, he served on the faculty of the Department of Electrical Engineering at IIT Delhi as a Professor.

He has published over 150 papers in international conferences and journals. He has served as the technical program chair for VLSI Design Conference and the VLSI Design and Test Symposium. He has also served as the member of the program committee for several conferences, including HiPC (High Performance Computing). He is the recipient of SIGDA student scholarship award, best paper award (VLSI Design conference) and best student paper award (VLSI Design conference). He is a senior member of IEEE, Fellow of the Indian Microelectronics Society, and current secretary of VSI.

Registration Fee

Before July 11, 2008		After July 11, 2007	
Professionals (Non- Members)	Rs.8,000/-	Professionals (Non- Members)	Rs.9,000/-
Professionals (VSI/ IEEE members)	Rs.7,000/-	Professionals (VSI/ IEEE members)	Rs.8,000/-
Students/Faculty (Non-members)	Rs.6,000/-	Students/Faculty (Non-members)	Rs.7,000/-
Students/Faculty (Members of VSI/ IEEE)	Rs.5,000/-	Students/Faculty (Members of VSI/ IEEE)	Rs.6,000/-

The registration fee includes registration material, softcopy of notes, lunch and refreshments.

Mode of Payment: Demand Draft, drawn in favor of **"VLSI Society of India"** payable at Bangalore.

Please also register using the online registration form at **http://vlsi-india.org/vsi/activities/reg.shtml** apart from sending the filled hardcopy of registration form. Spot-registration subject to availability at the after deadline rates against DD or Cash.

Digital Circuits Test and Design For Test

1. Introduction
2. CAD tools
3. Logic Test - Typical Fault Models
4. Advanced Faults Models
5. Design for Test
6. Logic BIST
7. Memory Test
8. Test Compression
9. Fault diagnosis
10. Industrial Case Studies

1. Introduction

1. Defects in DSM circuits
2. Systematic, Parametric vs. Random Defects
3. Yield and quality requirements
4. Objectives of digital testing
5. Relationship between defect coverage and DPM
6. Quality of test versus yield
7. Different phases and components of test
8. Factors affecting test

2. CAD tools

1. Logic simulators
2. Fault simulators
3. Test pattern generators
4. Scan insertion tools
5. Logic BIST
6. Memory BIST
7. Cost of test and test data compression

3. Logic Test - Typical Fault Models

1. Relation between defects and fault models
2. Measures – fault coverage, test coverage, test efficiency, etc.
3. Stuck-at Fault Model
4. Test pattern generation/fault simulation
5. Static and dynamic compaction
6. Delay fault models – transition, path-delay and inline resistance fault models
7. Launch off shift versus launch off capture
8. Transistor stuck-open faults, Transistor stuck-on faults
9. Industrial experience with at-speed tests
10. Iddq test sets
11. Effectiveness of Iddq tests on nanometer designs

4. Advanced Faults Models

Section A:

1. Bridging Faults
2. Targeting Bridging Faults – n-detect test sets
3. Test Generation for Bridging Faults
4. At-speed test application
5. False and multi-cycle paths
6. Avoiding hold-time violations during ATPG
7. Timing-aware ATPG
8. Propagation delay fault model
9. Validating data hold times
10. Test pattern ordering

Section B:

11. Power dissipation in scan based test
12. Power reduction – hardware based approaches
13. Software based methods – Weighted Switching Activity (WSA)
14. Capture cycle switching reduction
15. Reducing switching activity for scan load/unload
16. Results for industrial circuits

5. Design for Test

1. Scan designs – a mux-D based scan cell
2. How scan works?
3. DRC rule checks – uncontrollable clocks, etc.
4. Scan and its benefits
5. Enhanced scan architecture for at-speed tests
6. Scan-enable signal, pipelined scan-enable signal for at-speed test
7. Slow shift/fast capture
8. Enhanced scan architectures
9. Power conscious test techniques, test architectures

6. Logic BIST

1. Requirements for implementing BIST
2. Pattern Generation - Linear Feedback Shift Register
3. Characteristics of pseudo-random patterns
4. Output Compaction – Multiple Input Signature Register
5. Aliasing probability
6. Creating a BIST ready design
7. Handling of X-states
8. Handling of buses with multiple drivers
9. Feedback loops, latches
10. Random Pattern Resistant Faults
11. Test Points – improve controllability and observability
12. Overall Logic BIST Architecture
13. Boundary scan and BIST
14. A typical BIST session
15. Fault simulation and signature calculation
16. ATPG supplement patterns
17. Logic BIST diagnosis flow
18. Direct diagnosis from MISR signatures

7. Memory Test

1. Different fault models for memories
2. Conventional memory test algorithms
3. Advanced memory test algorithms
   - Address decoder open tests
   - Byte write-enable mask tests
   - Multi-port memory tests
4. Memory test techniques
   - Direct Access
   - Memory BIST
   - Macro Test
5. Typical Memory BIST Architecture
6. Methods for output evaluation
7. Typical address generators
8. Memory BIST collar
9. At-speed test application
10. Shared controllers – different test configurations
11. Memory diagnosis
12. Memory repair for yield improvement
13. E-fuse based memory repair
14. Memory BIST through JTAG interface
15. Localized address/data generation
16. Programmability – algorithm specification, selection
17. Field Programmable memory BIST
18. Macro Test – test small memories via scan vectors
19. At-speed test application using Macro Test

8. Test Compression

1. Conventional scan test – how does it work?
2. ATE costs for scan vector application
3. Test costs – data volume and scan test application time
4. Scalability of scan based solution with increasing design complexity
5. Requirements for a good compression scheme
6. Conventional scan and ATPG process
7. Scope for data volume reduction during ATPG
8. Non-embedded forms of compression
9. State of the art decompression techniques
10. Stimuli repetition, stimuli conversion, and stimuli replication
11. Stimuli encoding
12. Reseeding of LFSRs
13. Continuous Flow Decompression
14. Ring generators
15. Encoding capacity
16. Embedded Deterministic Test (EDT) Architecture
17. Advantages of using EDT - example
18. Test response compaction – requirements?
19. Time and Space compaction
20. State of the art compaction techniques
21. Selective compactor
22. Handling of X-states and aliasing
23. Finite memory compactors - convolutional and block compactors
24. Advanced compression techniques – how one can achieve very high compression?
25. Power reduction in compression based methods
26. Modular EDT architecture
27. Burn-in test requirements

9. Fault diagnosis

Section A:

1. Detection vs. Diagnosis; goals of diagnosing chip failures
2. Diagnosis at different levels – chip, board, system
3. Scan chain diagnosis
4. Logic diagnosis – methods
5. Fault dictionaries
   - Effect-Cause or Simulation Based Methods
6. Diagnostic resolution
7. Logic diagnosis procedures
8. Effect of compression on diagnosis
9. Direct diagnosis algorithms
10. Industrial case studies for diagnosis

Section B:

11. Current motivations for DFT and test
12. Design, test, and diagnosis flow
13. Current methods for yield learning
14. Defect based testing
15. Fault models based on physical data
16. Mapping from logical faults to physical defects
17. Closing the yield learning loop

10. Industrial Case Studies

1. SOC Design/test use
2. SOC test methodology and flow
3. Test re-use
4. IEEE 1500 and how it facilitates test reuse
5. Others…

August 11, 12 and 13	August 14
Dr. Nilanjan Mukherjee and **Prof. Sudhakar Reddy** ➢ Introduction ➢ CAD Tools ➢ Logic Test – Basics ➢ Logic Test ➢ Advanced Fault Models ➢ Power Aware Test ➢ DFT ➢ Logic BIST ➢ Memory Test ➢ Test Compression ➢ Fault Diagnosis	**Dr. C.P.Ravikumar** **Industrial Experiences** ➢ Test compression techniques ➢ At-speed testing techniques for SoC ➢ Signal integrity issues in Test ➢ Power issues in Test

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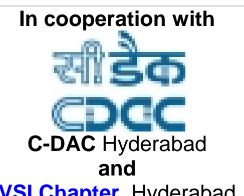
http://vlsi-india.org/vsi **VLSI Society of India**	August 11-14, 2008, Hyderabad, India **Venue: Hotel Green Park** Greenlands, Begumpet, Hyderabad, Tel : 091 - 040 - 66515151, 23757575 **Green Park - Hyderabad**	 **C-DAC** Hyderabad **and** **VSI Chapter**, Hyderabad

REGISTRATION FORM

Name of the participant:

(Please use block letters. The certificate will be made in this name)

Category: Tick appropriate	Industry Member (Non-VSI)	☐	Member of:	Membership No:
	VSI/ IEEE member	☐	VSI/ IEEE Membership No: Membership expiry date:	
	Academic/governmental organization from India (Non-VSI)	☐	Member of:	Membership No:
	Academic/governmental organization from India (VSI/ IEEE member)	☐	VSI/ IEEE Membership No: Membership expiry date:	
If you are a student, mention Semester/Year:				
Contact Address: **(Provide permanent mailing address)**	**Designation:** Student ☐ Faculty ☐ Industry ☐ Other ☐ **College/ Company:** **Permanent address:**			
E-mail: (Compulsory) (also provide alternate mail id)				
Background in VLSI: (Courses/Reading/Projects)				
Details of DD enclosed	DD Number			
	Drawn on Bank		Dated	

Your background and expectations from the workshop:

Signature

After completing the registration form, mail it with the DD to the following address:

Mr. Gopal Naidu
Treasurer, VLSI Society of India
Finance Department
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park
C.V. Raman Nagar, Bangalore 560093
vsiaccounts@vlsi-india.org

Please also enter details online at
http://vlsi-india.org/vsi/activities/reg.shtml

- Please prepare the DD for "**VLSI Society of India**" payable at **Bangalore**.
- On the back of the DD, please write, "**Short course on DCT-DFT, Hyderabad**".
- Cancellation requests must be received at least 2 weeks in advance. A processing fee of Rs.1000/= will be charged against cancellation made 2 weeks in advance. No refund will be made on cancellations made later.
- Substitute participants are permitted only if intimation is provided 2 weeks in advance.
- Queries may please be sent to: vsisecy@vlsi-india.org
- Seats are limited. Spot Registration is strictly by DD or cash payment subject to availability

Note:

- Course fee includes registration material, lunch and refreshments.
- VSI/ IEEE Members must have renewed membership to be eligible.
- Transport and stay arrangements are the responsibility of the participants.
- Registration can be transferred to a colleague with intimation 15 days prior to the event.
- Registration begins at 8.30 AM, Course schedule is from 9.00 AM to 5.00 PM.
- DD Acknowledgement from VSI through mail confirms registration.