Updated August 28, 2007

Final Program

11th IEEE VLSI Design and Test Symposium

http://vlsi-india.org/

August 8 – 11, 2007

Saha Institute of Nuclear Physics Convention Centre, Salt Lake

Kolkata, India

Sponsored by

VLSI Society of India

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VLSI Design and Test Symposium VDAT http://vlsi-india.org

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In cooperation with

Institute of Radio Physics and Electronics, Calcutta Univ.

Dept. of E & TCE, Jadavpur University

Indian Statistical Institute, Kolkata

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Tracks in VDAT Symposium:

Day 1-2 (August 8 and 9): The advance technical program includes

- 52 peer-reviewed technical paper presentations
- 19 poster papers, a panel discussion
- 5 Invited Talks
- 4 Keynote addresses and a Banquet talk.
- 8 Embedded Tutorials

The program is divided into 3 tracks.

- A track on **High-Level Design** will focus on System Level Design and Synthesis, Microarchitecture, Embedded Systems, Co-Design, Core-Based Designs, High-Level Synthesis, Logic Synthesis, Memory Synthesis, and FPGA Synthesis.
- A track on **Physical Design and VLSI Technology** will focus on Physical Design and Technology and Process-Related Aspects of Integrated Circuits. It will also discuss issues on Optoelectronic Devices and Circuits, MEMS, Deep Submicron and Nanometer Devices and Circuits.
- A track on **Testing and Verification** will focus on issues related to Testing, Testability and Verification of Digital Designs, Memories, Analog and Mixed-Signal Designs.

You may register for VDAT using the registration form enclosed. This registration also entitles you to attend the VLSI Education Day (Aug 10). Participants of VDAT may also wish to attend the One-day workshop on Nanotechnology on August 7, 2007 being organized at the Indian Statistical Institute, Kolkata at no extra charge – details will be announced shortly. You should also enter your registration details at our website to receive a confirmation from us.

Day-3 (August 10): VLSI Education Day includes a Keynote talk, 2 Invited Talks, 3 Embedded Tutorials and panel discussions related to VLSI education in India.

Day-4 (August 11): The following tutorials will be held on August 11, 2007 at the **Institute of Radio Physics and Electronics, Calcutta Univ.** You may register either for track T1, T2 or T3 shown below. Please note that registration for VDAT2007 and Tutorials are separate.
Those registering for T1 may also attend T3 optionally. T3 registrants can also attend the morning session of T1.

T1: Analog Design and BioChips

Low Power Design Technique in Analog And Mixed-Signal Design

Dr. Chetan Parikh, DAIICT and **Dr. Nagendra Krishnapura**, IIT Madras

Design and test of Microfluidic Biochips

Dr. K. Chakrabarty, Duke University, USA

T2: System-on-Chip Test

Manufacturing test solutions for System-on-chip Integrated Circuits

Dr. E. Larsson (Linkoping University, Sweden) and **Dr. K. Chakrabarty** (Duke University, USA)

Compression, Delay test and Diagnosis: Ensure High quality, Low cost and Quick yield Ramp of Nanometer ICs

Navneet Kaushik, **Shaleen Babu** and **Sameer Chillarige** (Cadence)

T3: Power Management

Power Management Circuits Design & Applications

Amit Patra and **S. Mukhopadhyay**, IIT Kharagpur, **Ram Anant** and **S. Venkatraman**, TI India

Red Marked Papers were not presented at the symposium

Day-1 (August 8, 2007) – Wednesday			
08.00 AM – 09.00 AM	**Registration and Breakfast**		
09.00 AM - 09.30 AM	**Inauguration**		
09.30 AM - 10.30 AM	Keynote-1 ***Dr. Debesh Das***, *IT Minister, WB and Professor, Jadavpur University, Kolkata* **The Emergence and the Status of VLSI Activities in India** Keynote-2 ***S Janakiraman***, *ISA Chairman and President R& D Services Mindtree Consulting* **Establishing the Semiconductor & Electronics Ecosystem: Opportunities and Challenges** **Chair Person:** ***Vishwani Agrawal***, *Auburn University* **Venue:** J.C. Bose Hall		
10.30 AM – 11.00 AM	**Tea Break**		
	Session 1A-1 **TECHNOLOGY-1** **Chairperson:** ***Hiranmay Saha***, *Jadavpur University* **P.C. Mahalanabis Hall**	**Session 1B-1** **EDA-1** **Chairperson:** ***Swapan Sen,*** *Saha Inst of Nuclear Physics* **J.C. Bose Hall**	**Session 1C-1** **DFT-1** **Chairperson:** ***C P Ravikumar***, *TI* **S.K. Mitra Hall**
11.00 AM - 01.00 PM	**Challenges Posed to the State of the art Device Simulators in Nanoscale Regime** Embedded tutorial (1 hr) *Shubhakar K, Biswajit Ray and* ***Santanu Mahapatra****, Indian Institute of Science, Bangalore*	**Design for Manufacturability: What Lies Ahead?** ***Vijay S. Patri****, Magma Design Automation* Embedded Tutorial (1 hr)	**Robust System Design for Scaled CMOS and Emerging Nanotechnologies.** ***Subhashis Mitra****, Stanford University* Invited Talk
	A Simulation based Study and Analysis of Double Gate Tunnel FET Performance for Low Standby Power Applications ******Nayan Patel****, Santanu Mahapatra, IISc, Bangalore* Regular	**An Algorithm for Resistance Extraction and Current Density Profiling of Lateral Power MOSFETs** ******Baidurya Chatterjee****, Syamantak Das, Amit Patra, IIT Kharagpur; Samrat Ray, Cadence Design Systems, Noida* Regular	**Layout-Aware Illinois Scan Design for High Fault Coverage** ******Shibaji Banerjee****, IIT, KGP* Regular
	Multilevel Pyramidically Wound Symmetric Spiral Inductor *Genemala Haobijam,* ***Roy Paily*****, IIT, Guwahati* Short	**An Error Comparison Scheme for Design Rule Checking Flows** ******Dibyendu Goswami****, Swami Gangadharan, Intel* Regular	**Compression-Power Trade-off in Dictionary based Test Data Compression** ******Chandan Giri****, Nikhil Reddy Cheruku, Santanu Chattopadhyay, IIT Kharagpur* Regular
	Floating Gate Interferences on Vth Distribution In Eight Level High Density Flash Memory ******Roy Paily****, Vikas Badam, IIT Guwahati; Yajun Ha, National University of Singapore* Short	**Delay Clock Methodology for Timing-Performance Improvement of Designs on FPGAs** ******Kamakoti Veezhinathan****, IIT Madras* Regular	**Fault Diagnosis in Reversible Circuits** ******Bikromadittya Mondal****, BPPIMT; Susanta Chakraborty, Bengal Engg. and Science University; Bhargab Bhattacharya, Indian Statistical Institute, Kolkata* Short
01.00 PM - 02.00 PM	**Lunch**		
	Session 1A-2 **ANALOG DESIGN-1** **Chairperson:** ***D. Mukhopadhyay,*** *Jadvpur University* **P.C. Mahalanabis Hall**	**Session 1B-2** **EDA-2** **Chairperson:** ***P. Dasgupta***, *IIM Calcutta* **J.C. Bose Hall**	**Session 1C-2** **DFT - 2** **Chairperson:** ***D. Roy Choudhury***, *IITKGP* **S.K. Mitra Hall**
02.00 PM – 03.30 PM	**Design of Synchronous Buck Converter Employing an Adaptive Zero Voltage Switching for Ultra Low Power Systems** ******Sandeep Mehra*** *and Bhardwaj Amruthur, Indian Institute of Science* Short	**The Next Step in the SoC Design Automation** ***Manikandan Panchapakesan*** *and Ramchandra V, NXP Semiconductors* Embedded Tutorial (30 minutes)	**Using Hierarchy in Design Automation: The Fault Collapsing Problem** ******Vishwani Agrawal****, Auburn University; Raja Sandireddy, Intel Corporation* Regular
	A 2.4 GHz Low-voltage CMOS Low Noise Amplifier with 32dB Gain *Anuradha Ray, ST Microelectronics;* ***Chetan Parikh*****, DA-IICT* Short	**Crosstalk Noise Analysis Tool and Development of an Automated Spice Correlation Suite to Enable Accuracy Validation** ******Venugopal Chakravarthy****, S J College of Engg; Jagannath Rao, SJ College of Engg* Regular	**Testing Droop Faults in Full Scan Circuits** ******Debasis Mitra****, Bengal Engineering and Science University, Shibpur, Howrah.; Ashish Nigam, ; Sandeep Dey*, Susmita Sur-Kolay, Bhargab Bhattacharya, Indian Statistical Institute, Kolkata* Regular
	Design and implementation of a 14-bit 200 MSPS Current Steering DAC using GM/ID Method *Ramasamy Srinivasan,* ***Venkataramani Balasubramanian*****, Sreekanthbabu Nukaraju, NIT Tiruchirappalli* Short	**Voltage Scalable Statistical Gate Delay Models Using Neural Networks** ******Bishnu Das****, Bharadwaj Amrutur, Indian Institute of Science; H.S.Jamadagni, CEDT, IISc, Bangalore* Regular	**A New Approach for Testing of Digital Modules in Mixed Signal VLSI Circuits** ******Santosh Biswas****, IIT Kharagpur* Regular

02.00 PM – 03.30 PM	**Low-power High Slew-rate Adaptive Biasing Circuit for CMOS Amplifiers** ***Chetan Parikh****, DA-IICT; Narayana Rao, DA-IICT, Gandhinagar* Short	**Fast I/O Pad Placement in FPGAs** ****Debasri Saha****, Pritha Banerjee, Susmita Sur-Kolay, Indian Statistical Institute* Short	**Detection of Single Stuck-at and Bridging Faults in Cluster-based FPGA Architectures** ****Hafizur Rahaman****, Bengal Engg. and Science University* Short
	Design of High Performance Current Steering DAC using Pattern Search Algorithm *Sreekanthbabu Nukaraju, Ramasamy Srinivasan,* ***Venkataramani Balasubramanian****, NIT, Trichy* Regular	**Crosstalk Analysis for a CMOS Gate Driven Coupled Interconnects** ****Brajesh Kaushik****, Sankar Sarkar, MITS, Sikar; Rajendra Agarwal, Ramesh Joshi, IIT, Roorkee* Regular	**Genetic Algorithm based Test Scheduling for Network-on-Chip** ****Santanu Chattopadhyay****, Mahalakshmi Satti, Santanu Kundu, IIT Kharagpur* Short
03.30 PM – 04.00 PM	**Break**		
04.00 PM – 05.30 PM	**Panel Discussion** **Moderator:** ***Srimat Chakradhar****, NEC Labs, USA*		
05.30 PM – 06.00 PM	**Break**		
06.00 PM – 07.00 PM	**Banquet Talk** **Convergence of Semiconductor Industry** ***Sreedhar Natarajan,*** *Emerging Memory Technologies* **Chairperson:** ***Susanta Sen****, Calcutta University*		
07.00 PM – 08.00 PM	**Entertainment**		
08.00 PM – 09.00 PM	**Dinner**		
End of Day-1			

Red Marked Papers were not presented at the symposium

Day-2 (August 9, 2007) – Thursday			
08.00 AM - 09.00 AM	**Registration and Breakfast**		
09.00 AM – 10.00 AM	**Keynote-3** ***Sumeet Agrawal**, Intel* **Modular Design: Industry perspective and open challenges** **Chair: *Bhargab B. Bhattacharya**, Indian Statistical Institute*		
10.00 AM - 10.30 AM	**Tea Break**		
	Session 2A-1 **LOW-POWER-1** **Chairperson: *S. Chattopadhyay**, IITKGP*** **P.C. Mahalanabis Hall**	**Session 2B-1** **SYSTEMS-1** **Chairperson: *P. Panda**, IITD*** **J.C. Bose Hall**	**Session 2C-1** **TEST AND VERIFICATION - 1** **Chairperson: *Partha Pratim Das**, Interra Systems, Kolkata*** **S.K. Mitra Hall**
10.30 AM - 12.30 PM	**Aggressive Leakage Management in ARM based system** ***Jayanta Lahiri**, ARM Embedded Technologies* Invited Talk (40 min)	**A Methodology for Creating Application Specific Processor Architectures** ***Prof. Anshul Kumar**, IIT Delhi* Invited Talk (40 min)	**Low power verification** ***Sathyam Pattanam**, Synopsys* Invited Talk (40 min)
	CV-based Analytical Modeling of Dynamic Power for 65nm CMOS Library Characterization ***B.P.Harish**, University Visvesvaraya College; Navakanta Bhat, IISc, Bangalore* Regular	**Dual Encoded Gray Coding Scheme** ***Salil Gadgil**, Texas Instruments; Senthilkannan Chandrasekaran, Texas Instruments* Regular	**Debugging Assume-Guarantee Specification for Compositional Verification** ***Anindyasundar Nandi**, Interra Systems India Pvt Ltd; Bhaskar Pal,; Pallab Dasgupta, IIT Kharagpur* Regular
	A Novel Efficient Power Optimization Method for Off-Chip Memory Access using Differential Memory Addressing ***Sajal Das**, Texas Instruments, Bangalore* Regular	**Incremental Connectivity Extraction for Large VLSI Layouts** ***Akash Agrawal**, IIIT Hyderabad* Short	**Formal Verification of Pipelined Read-Modify-Write Logic by GSTE** ***Subir Roy**, Texas Instruments India Pvt Ltd; Srikanth Reddy, Bharadwaj Amrutur, IISc, Bangalore* Short
	Leakage Modelling of Logic Gates Considering The Effect of Input Vectors ***Janakiraman Viraraghavan**, Bishnu Das, IISc, Bangalore; Vish Vishwanathan, TI; Bharadwaj Amrutur, IISc, Bangalore* Regular	**Latency Optimized AES-Rijndael with Flexible Mode of Operation** ***Monjur Alam**, Santosh Ghosh, IIT - Kharagpur; Debdeep Mukhopadhaya, IIT - Madras; Dipanwita Roy Chowdhury,; Indranil Sen Gupta, IIT- Kharagpur* Regular	**An Efficient Implementation of Testbench for Verification of Configurable Host Controller IP Addressing Mobile Storage Applications** ***Pusuluri Giri Kumar**, Synopsys (India) Pvt Ltd* Short
		On the Realizability of Specifications having Auxiliary State Machines and GR(1) LTL ***Ansuman Banerjee**, Pallab Dasgupta, Partha Chakrabarti, IIT Kharagpur* Regular	**Scenario Driven Test Case Generation for Functional Verification of Pipelined Processors** ***Subrat Panda**, Venu Gopal Kasturi, Partha Chakrabarti, IIT Kharagpur* Regular
12.30 PM - 01.30 PM	**Lunch**		
01.30 PM – 02.30 PM	**Keynote-4** ***Vivek Raghavan**, General Manager and VP Product Development* **Creating a successful EDA product: An industry veteran's perspective** **Chairperson: *S. Sur-Kolay**, ISI***		
	Session 2A-2 **LOW-POWER-2** **Chairperson: *Anshul Kumar,** IITD* **P.C. Mahalanabis Hall**	**Session 2B-2** **SYSTEMS-2** **Chairperson: *Hafizur Rahaman**, BESU*** **J.C. Bose Hall**	**Session 2C-2** **MEMS-TECHNOLOGY-1** **Chairperson: *P.K.Basu**, University of Calcutta*** **S.K. Mitra Hall**
02.30 PM – 03.45 PM	**Leakage and Switching Power Minimization with Area Trade-off in Multiplexer Based Circuit Synthesis** ***Sambhu Pradhan**, Santanu Chattopadhyay, IIT Kharagpur* Short	**A Transformation Based Method for Formal Analysis of Hybrid Systems** ***Jairam Sukumar**, Subir Roy, Texas Instruments, Bangalore; Navakanta Bhat, IISc, Bangalore* Regular	**Fabrication of MEMS PZR Accelerometer for Automobile Application** ***Ravindra Mukhiya**, E&ECE, IIT-Kharagpur* Regular
	A Novel Toggle less, LUT-Less Low Power Distributed Arithmetic (DA) Architecture for FIR Filter ***Uma Rajaram**, Augusta Sophy, Easwari Engineering College* Short	**Hybrid Masked Karatsuba Multiplier for GF (2^{233})** ***Debdeep Mukhopadhyay**, IIT Madras* Short	**Bulk-Micromachining for MEMS Accelerometer using 25% WT. TMAH** ***Ravindra Mukhiya**, E&ECE, IIT-Kharagpur* Short

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02.30 PM – 03.45 PM	**A Core Power Pad Planner for Wirebond SoCs** **Jairam Sukumar, Udayakumar H, Texas Instruments, Bangalore; Rajat Chopra, Interra Systems; Kousik Mukherjee, Interra Systems* Short	**Priority Queue based LRU Models for Associative Cache** **Vijayalakshmi Seshadri, Airvana Networks India Pvt Ltd* Short	**Design, Modeling and Simulation of High Performance RF MEMS Switch for Phase Shifter Applications** **Avra Kundu; Swati Majumdar; Bhaskar Gupta; Hiranmay Saha, Jadavpur University* Regular
	Design of an Application Specific Low-Power High Performance Carry Save 4-2 Compressor **Anup Dandapat, Partha Bose, Sayan Ghosal, Pikul Sarkar, Animesh Biswas, D Mukhopadhyay, Jadavpur University* Short	**A New Spice Simulator for Single Electron Transistor Based Integrated Circuits** **Biswajit Ray, Ashish Pal, Saptarshi Das, Santanu Mahapatra,IISc, Bangalore* Regular	**Characterization of Universal Nand-Nor-Inverter QCA gate** **Biplab Sikdar, Bibhas Sen, Bengal Engg and Science University* Regular
03.45 PM - 04.00 PM	**Break**		
	Session 2A-3 **SYSTEMS-3** **Chairperson: *Chetan Parikh*, DA-IICT** **P.C. Mahalanabis Hall**	**Session 2B-3** **CIRCUITS - 1** **Chairperson: *Vineet Sahula*, MNIT Jaipur** **J.C. Bose Hall**	**Session 2C-3** **DFT VERIFICATION** **Chairperson: *Pallab Dasgupta*, IITKGP** **S.K. Mitra Hall**
04.00 PM – 05.45 PM	**Design of Low Power & Robust Networks on Chip through Novel Coding Schemes** ***Partha Pratim Pande,** Washington State University* Invited Talk – 1 hr	**A Power Efficient Carry Break Adder Implementation using Input Pattern Based Area Reduction Technique for Adder Structures** **Krashna Nand Mishra, DA-IICT, Ahmedabad; Subash Chandra Bose, CEERI, Pilani* Short	**Formal verification of DFT logic and their integration in SoCs – practices, issues and challenges** ***Subir K. Roy**, Texas Instruments, Bangalore; **A.S. Nandi**, **B. Mittra** Interrasystems, Kolkata* Embedded Tutorial
	A Lifting based Reconfigurable forward and Inverse Discrete Wavelet Transform Architecture for JPEG2000 *Yogesh Inamdar; **Ramesh Kini***, N.I.T.K., Surathkal* Short	**Area Efficient Bit-Serial Architecture for Polynomial Basis Multiplication over Galois Fields GF(2^m)** **Hafizur Rahaman, Bengal Engg. and Science Univ; Prasenjit Ray, Debasis Mitra, Amit Datta, School of VLSI Technology, Bengal Engineering and Science University, Shibpur* Short	
	MOTSOC: Mesh of Tree based Network-on-Chip Design A New Interconnection Structure for SOCs **Santanu Kundu, Santanu Chattopadhyay, Mahalakshmi Satti, IIT Kharagpur* Short	**A Bus Encoding Technique for On-Chip Propagation Delay Minimization** *Nallamothu Satyanarayana, Adams Engineering College; A Vinaya Babu, JNTU Hyderabad; **Madhu Mutyam***, IIIT Hyderabad* Short	
	State Encoding Targeting Low Area And Low Power FSM Synthesis **Santanu Chattopadhyay, Saurabh Chaudhury, IIT Kharagpur; Krishna Sistla* Regular	**Design Approach for Standard Single Ended Input Output Buffer in 65nm Process** ***K S Raghunathan*** Embedded Tutorial (1 hr)	
05.45 PM – 06.00 PM	**Break**		

Red Marked Papers were not presented at the symposium

	Poster Session		
	Session 2A-4 **CIRCUITS - 2** **Chairperson: *Baidya Nath Ray,*** *Bengal Engineering and Science University* **P.C. Mahalanabis Hall**	**Session 2B-4** **ANALOG DESIGN - 2** **Chairperson: *Bharadwaj Amrutur***, *IISc, Bangalore* **J.C. Bose Hall**	**Session 2C-4** **TEST AND VERIFICATION - 2** **Chairperson: *Susanta Chakraborty***, *Bengal Engg and Science University* **S.K. Mitra Hall**
06.00 PM – 07.00 PM	**A Novel Approach for Power Pad Layout generation** ***Venkat Vallapaneni***, *Raghunatha Lakkireddy, Sireesha LNVS Tulluri, Srinivasa Gandi, Agere Systems*	**Power Supply Detection Circuit** ****Dharmaray Nedalgi***, *and Mukesh Nair, NXP Semiconductors*	**Co-simulation: Verification Advantage with PCI Express Endpoint SystemC Model** *Aditya Ayre,,* ***Aniket Deshpande****; *Vishal Rustagi, CDAC-Pune*
	A Double-Pulsed Latch Flip-Flop ****Navaram Kumar***, *VNIT; Rajendra Patrikar, and Kishore Kulat VNIT Nagpur*	**VCO Phase Noise Improvement Techniques** *Ravi Kumar, IBM;* ***Narendra Bolabatin****, *Qualcorelogic; Eapen Abraham, IBM*	**Case study: Reducing Run time of Volume Diagnosis by Using Reduced Pattern Set and Truncated Failure Log** ****Dhiraj Maheshwari***,; *Ravi Dasari, Mentor Graphics*
	Design of Flip-Flops with Low Setup and Hold Times across Process Variations ****Pratap Das***, *Bharadwaj Amrutur, Indian Institute of Science; Sridhar J., TI India*	**Development of an FPGA based Smart Computing System for Clinical Diagnosis with On-board Wireless Communication Interfacing** ****Shubhajit Roy Chowdhury***, *Hiranmay Saha, Jadavpur university*	**Formal Verification of a Fast DMA Controller: A case study** *Anindyasundar Nandi,,* ***Bijitendra Mittra****, *Interra Systems India Pvt Ltd; Subir Roy, Prohor Chowdhury,Texas Instruments, India*
		Design and Simulation of Integrated VCO for SMART Nanoporous Silicon Based Biosensors ****Chirasree Roy Choudhury***, *Subhashis Sinhababu, Bengal Engineering and Science University, Shibpur*	
End of Day-2 of Symposium			

Red Marked Papers were not presented at the symposium

<table>
<tr><td colspan="4">Day-3 (August 10, 2007) – Friday
VLSI Education Day</td></tr>
<tr><td>08.00 AM - 09.00 AM</td><td colspan="3">Registration and Breakfast</td></tr>
<tr><td>09.00 AM - 10.00 AM</td><td colspan="3">Keynote-5
Jagdish Rao, Texas Instruments Bangalore
Predictable Physical Design Closure in the Nanometer Era - An Industry Perspective
Chairperson: Jayanta Lahiri, ARM Embedded Technologies</td></tr>
<tr><td>10.00 AM – 10:30 AM</td><td colspan="3">Tea Break</td></tr>
<tr><td></td><td>Session 3A-1
Physical Design
Chairperson: Indranil Sengupta, IIT KGP
P.C. Mahalanabis Hall</td><td>Session 3B-1
VLSI Education
Chairperson: Dinesh Sharma, IIT Bombay
J.C. Bose Hall</td><td>Session 3C-1
Low Power Test
Chairperson: S. Majumder, IIIT
S.K. Mitra Hall</td></tr>
<tr><td>10:30 AM – 11.30 AM</td><td>Invited Talk</td><td>Invited Talk</td><td>Addressing Test Power Issues in Digital CMOS Circuits
Srivaths Ravi, Texas Instruments
Embedded Tutorial</td></tr>
<tr><td>11.30 AM – 01.00 PM</td><td>Game Theory and its Application to VLSI Physical Design
Parthasarathi Dasgupta, IIM Calcutta
Embedded Tutorial</td><td>Research Scholar Forum
Research Scholars must send their proposals to vsisecy@vlsi-india.org</td><td>Strategies for power reduction during VLSI circuit testing
S. Chattopadhyay, IIT Kharagpur
Embedded Tutorial</td></tr>
<tr><td>01.00 PM - 02.00 PM</td><td colspan="3">Lunch</td></tr>
<tr><td></td><td colspan="2">Poster Session</td><td rowspan="2">Session 3C-2
VSI Meeting – Proposals from colleges for conducting future events
S.K. Mitra Hall</td></tr>
<tr><td></td><td>Session 3A-2
LOW POWER - 3
Chairperson: Aloke Das, Intel
P.C. Mahalanabis Hall</td><td>Session 3B-2
DESIGN TECHNIQUES
Chairperson: Biplab Sikdar, Bengal Engg and Science University
J.C. Bose Hall</td></tr>
<tr><td>02.00 PM - 03.00 PM</td><td>Power Optimized Machine Code Generation for an Application Specific Instruction Set Processor (ASIP) for Hindi Text to Speech Synthesis
*Atanendu Mandal, CEERI</td><td>Modified Data Encoding Circuit for Asynchronous FIFO Design
*Roy Paily, IIT Guwahati; Krishna Chaitanya, IIT Guwahati</td><td rowspan="5">VLSI Society of India invites proposals from its member organizations to conduct events in 2007-2008. Proposals must be sent in the format prescribed on the website. Continuing events of VSI include
(a) VLSI Design Conference (proposals for 2010 or later)
(b) VDAT Symposium (proposals for 2008 or later)
(c) Design Verification Methodologies (Proposals for 2008 or later)
(d) Workshop on Low Power Design (Proposals for 2008 or later)
(e) Workshop on Electronic System Level Design (Proposals for 2008 or later)
(f) Workshop on Interconnect Design and Variability (Proposals for 2008 or later)
(g) Proposals for tutorials or other events
For proposals that are sent earlier and already approved, time will be provided to organizers to present their proposals and seek participation. Proposals can be sent to ravikumar@vlsi-india.org</td></tr>
<tr><td></td><td>Implementation of SPIHT Codec in Stratix-II
*Gunvanta Mate, Kishore Bachina; K Ramesh, CRL-BEL; J. Anbuselvi</td><td>Design and Simulation of a CMOS Instrumentation Amplifier for signal conditioning of MEMS based Piezoresistive low Pressure Sensor
*Niteen Futane ; Shubhajit Roy Chowdhury,, Jadavpur Univerity; Chirasree Roy Choudhury,. BESU; Hiranmay Saha, Jadavpur University</td></tr>
<tr><td></td><td>FPGA Implementation of Low Power ASU Multiplier
*Rahul Badghare,; Sanjiv Mangal, Raghvendra Deshmukh,; Rajendra Patrikar, VNIT, Nagpur</td><td>Effect of Inductance on Wire-Sizing the Global Interconnect in VLSI Circuits
*Ashwani Kumar, Surender Soni, NIT Hamirpur; Ashok Kumar</td></tr>
<tr><td></td><td>Improved Reversible Logic Implementation of Decimal Adder
*Rekha James, CUSAT; Shahana T K, CUSAT; K. Poulose Jacob, CUSAT; Sreela Sasi, Gannon University</td><td>Circuit Prospects Of DGFET: A Variable Gain Differential Amplifier With Current mirror Load
*Srimoyee Sen, Urmimala Roy, Chandan Sarkar, Jadavpur University; Chaitanya Kshirsagar; Navakanta Bhat, ECE, IISc, Bangalore</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>03.00 PM - 03.30 PM</td><td colspan="3">Tea Break</td></tr>
<tr><td>03.30 PM - 05.00 PM</td><td colspan="3">Panel
Taking VLSI Education in India to the Next Level – What? Who? How? And When?
VLSI education has come a long way in the last ten years. Today, many colleges offer M.Tech programs in VLSI. B.Tech level courses in VLSI are being offered in many colleges. There are many Ph.D. scholars working in the area of VLSI. The panelists will take a fresh look at VLSI Education in India and debate how to take it to the next level.
Moderator: C.P.Ravikumar, Texas Instruments India
Panelists: N.S. Murty, NXP Semiconductors and others</td></tr>
<tr><td colspan="4">End of Day-3 – Symposium</td></tr>
</table>

Tutorials on Day-4 (August 11, 2007) – Saturday **Venue:** Institute of Radio Physics and Electronics, University of Calcutta 92 A. P. C. Road, Kolkata - 700 009			
08.00 AM - 09.00 AM	**Registration and Breakfast**		
	Session 4A-1 **Tutorial T1** **ANALOG DESIGN AND BIOCHIPS**	**Session 4B-1** **Tutorial T2** **SYSTEM-ON-CHIP TEST**	**Session 4C-1** **Tutorial T3** **POWER MANAGEMENT**
09.00 AM - 11.00 AM	**T1-A** **Low Power Design Technique in Analog And Mixed-Signal Design** ***Chetan Parikh**, DAIICT and **Nagendra Krishnapura**, IIT Madras*	**T2-A** **Manufacturing Test Solutions for System-on-chip Integrated Circuits** ***E. Larsson**, Linkoping University, Sweden and **Krishnendu Chakrabarty** Duke University, USA*	
11.00 AM - 11.30 AM	**Tea Break**		
11.30 AM – 01.00 PM	Tutorial Continues	Tutorial Continues	
01.00 PM - 02.00 PM	**Lunch**		
02:00 PM – 03:30 PM	**T1-B** **Design and test of Microfluidic Biochips** **Krishnendu Chakrabarty**, Duke University, USA	**T2-B** **Compression, Delay test and Diagnosis: Ensure High quality, Low cost and Quick yield Ramp of Nanometer ICs** ***Navneet Kaushik**, **Shaleen Babu** and **Sameer Chillarige**, Cadence Design Systems*	**T3-B** **Power Management Circuits Design & Applications** ***Amit Patra** and **S. Mukhopadhyay**, IIT Kharagpur, **Ram Anant** and **S. Venkatraman** and **Biranchinath Sahu**, TI India*
03.30 PM - 04.00 PM	**Tea Break**		
04.00 PM – 05:30 PM	Tutorial Continues	Tutorial Continues	Tutorial Continues
End of Tutorials			

There are three tutorial tracks – T1, T2 and T3. You may register for any one of them. Please note that registration in VDAT Tutorial registration entitles you to course CD, lunch, and refreshment.
Please note that registration for the tutorials is separate – registration in VDAT does not automatically enroll you into a tutorial. You must clearly indicate which tutorial you wish to enroll for – T1, T2 or T3. Partial registration is not permitted. Use the attached registration form to register. You must also confirm your registration on our website to get an acknowledgement from us.
Those registering for T1 may also attend T3 optionally. T3 registrants can also attend the morning session of T1.

Symposium Committee

General Co-Chairs

C.P. Ravikumar, Texas Instruments India and **BB Bhattacharya**, Indian Statistical Institute

Technical Program Committee

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S Sur-Kolay, Indian Statistical Institute
Parthasarathi Dasgupta, IIM Calutta
D Mukhopadhyay, Jadavpur University

Registration Information:

- Registration permits you to participate in all the Technical sessions and Tutorials organized as part of the Symposium, and includes refreshments and lunch on all days.
- Please send your registration fee through a draft made out to "***VLSI Society of India***", payable at Bangalore**.**
- The draft must be sent to ***Mr. Nandagopal Chattopadhyay****, VDAT2007 Finance Chair, to the address mentioned below.*
- If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Foreign Currency or Credit Card payments.
- The current exchange rate is approximately 1 US dollar = 45 Indian rupees.
- Even those of you who plat to register on the spot are requested to communicate your desire to attend VDAT 2007 to **vdat07@gmail.com** with details of vehicle registration number (if any) and laptop number (if any). Without this, you may face difficulties during registration. Please mark the subject line of the mail as "Vehicle No." or "Laptop No."
- If you are registering for a tutorial, indicate the first and second preference of the tutorial. There are limited seats in each tutorial. If we cannot register you in the tutorial of your choice, we will refund the amount.
- A processing fee of Rs.500/- will be applied against all cancellations.

Symposium Registration Amount

	Fellow	Indian Faculty/ Student	Indian Industry VSI/ IEEE Member	All Foreign Participants	Others
Before June 30, 2007	Rs.1500/=	Rs.2500/=	Rs.6000/=	US$ 150.00	Rs.7000/=
After June 30, 2007	N/A	Rs.3000/=	Rs.7000/=	US$ 200.00	Rs.8000/=

Tutorial Registration Amount

Before June 30, 2007	Rs.1000/=	Rs.1500/=	Rs.2000/=	US$ 100.00	Rs.2500/=
After June 30, 2007	Rs.1500/=	Rs.2000/=	Rs.2500/=	US$ 125.00	Rs.3000/=

Correspondence address for Registration:
Mr. Nanda Gopal Chattopadhyay, Finance Chair, VDAT 2007
C/o: Interra Systems India (Pvt) Ltd.
2nd Floor, STP II Building, Salt Lake Electronics Complex, DN-53
Sector V, Bidhannagar, Kolkata 700 091, WB, India
vdat07@gmail.com

Event	Venue	Date	Participants
1st VDAT	Chennai	January 7, 1998	30
2nd VDAT	New Delhi	August 6-7, 1998	70
3rd VDAT	New Delhi	August 20-21, 1999	120
4th VDAT	New Delhi	August 25-26, 2000	150
5th VDAT	Bangalore	August 16-18, 2001	220
6th VDAT	Bangalore	August 29-31, 2002	300
7th VDAT	Bangalore	August 28-30, 2003	300
8th VDAT	Mysore	August 26-28, 2004	250
9th VDAT	Bangalore	August 10-13, 2005	320
10th VDAT	Goa	August 9-12, 2006	300

Information

*Please watch updates on VDAT at http://vlsi-india.org The idea behind the VLSI Design And Test (VDAT) Symposium is to promote Research and Development on all aspects of VLSI in India. This symposium is a forum for free discussion of hot and emerging topics in VLSI. It provides a meeting place for VLSI professionals working in India and abroad. We have been holding this event since 1998, and the participation in the event has steadily gone up every year. Until 2004, the event was called "**VLSI Design and Test Workshops**." The VLSI Industry in India and academic community working in the area of VLSI has provided immense support to the symposium.*

*VDAT is sponsored by the **VLSI Society of India**. Please consult http://vlsi-india.org/vsi/ for more information on VSI"s mission and goals. If you are unable to download the page, please send mail to vsisecy@vlsi-india.org for a softcopy of the application form. Consult http://www.vlsi-india.org/vsi/activities/ for updates on the activities of the VLSI Society of India. If you wish to become a member of the VLSI Society of India, you can download the form from http://vlsi-india.org/vsi/membership/.*

11th IEEE VLSI Design and Test Symposium

August 08 - 11, 2007, Kolkata, India

Saha Institute of Nuclear Physics, Convention Centre, 1/AF, Bidhannagar, Salt Lake, Kolkata - 64

Website: vlsi-india.org

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http://vlsi-india.org/vsi/

REGISTRATION FORM

Name of the participant: (Please use block letters.)

Category: (Tick appropriate)	Fellow	☐	VDAT 2007 Fellowship No:
	Faculty / Student: VSI/ IEEE member	☐	VSI/ IEEE Membership No:
	Indian Industry: VSI/ IEEE member	☐	VSI/ IEEE Membership No:
	Author	☐	Paper No/s:
	Foreign Participant	☐	
Address for Correspondence:	**Designation:** Student ☐ Faculty ☐ Industry ☐ Other ☐ **College/ Company Name:** **Permanent address:**		
E-mail: (Compulsory):			
Choice of tutorial: **T1** ☐ **T2** ☐ **T3** ☐ **T1**: Analog Design and Biochips; **T2**: System on-chip Test; **T3:** Power Management			Telephone:
Details of DD enclosed	Tutorial:		DD Number:
	Symposium:		Dated:
	Total Amount:		Bank:

Attend: Symposium ☐ Symposium+T1 ☐ Symposium+T2 ☐ Symposium+T3 ☐

T1 ☐ **T2** ☐ **T3** ☐ One-day Workshop on Nanotechnology ☐

Those registering for **T1** may also attend **T3** optionally. **T3** registrants can also attend the morning session of **T1**. Please refer advance program.

Signature

Tutorial Registration Amount		
T1, T2 or T3 Aug 11, 2007	*Before June 30, 2007*	*After June 30, 2007*
Fellow	Rs 1000	Rs 1500
Faculty/ Student	Rs 1500	Rs 2000
Indian Industry VSI/ IEEE Member	Rs 2000	Rs 2500
Foreign Participant	USD 100	USD 125
Others	Rs 2500	Rs 3000

Symposium Registration Amount		
August 8- 10, 2007	*Before June 30, 2007*	*After June 30, 2007*
Fellow	Rs 1500	N/A
Faculty/ Student	Rs 2500	Rs 3000
Indian Industry VSI/ IEEE Member	Rs 6000	Rs 7000
Foreign Participant	USD. 150	USD 200
Others	Rs 7000	Rs 8000

Mail the completed registration form and DD to the following address:

Mr. Nanda Gopal Chattopadhyay
Finance Chair, VDAT 2007
C/o: Interra Systems India (Pvt) Ltd.
2nd Floor, STP II Building
Salt Lake Electronics Complex, DN-53
Sector V, Bidhannagar,
Kolkata 700 091, WB, India

- *The DD to be made out to "**VLSI Society of India**" payable at **Bangalore, India**.*
- *The DD and form to be sent to the VDAT2007 Finance Chair, to Kolkata address mentioned on the left.*
- *You must also enter the above details electronically at our website to receive information from us regularly*
- *If an author is also a fellow recipient, please tick both.*
- *Queries regarding registration must be sent only to: vdat07-regn@vlsi-india.org*

Note:

Symposium registration fee includes registration material, lunch and refreshments on all the days.
If registering separately for Symposium and Tutorial, please submit separate forms for each. Transport and stay arrangements are the responsibility of the participants.
Those registering for T1 may also attend T3 optionally. T3 registrants can also attend the morning session of T1.
A One-day workshop **on Nanoscience and Biochips** is being organized on Aug 7, 2007 at the Indian Statistical Institute, Kolkata – Limited number of free registration is available on a first-come first-serve basis to those registering for VDAT2007 Symposium. For details, please contact: Susmita Sur-Kolay (ssk@isical.ac.in), or Sandip Das (sandipdas@isical.ac.in).

VSI Membership Form

For New Membership and renewals

VLSI Society of India

http://vlsi-india.org/vsi/

Registered Society under KSR Act 1960, Rule 1961

E-mail: **vsiaccounts@vlsi-india.org**, **vsisecy@vlsi-india.org**

New Members to affix photograph.

1. Existing Membership No: ☐☐☐☐ (Quote additional Old No. If any): ☐☐☐☐

Member (tick as applicable): ☐ **Student** / ☐ **Non-student** / ☐ **Corporate**

2. Your Name:

3. Your Profession/ Designation:

4. Your e-mail address:

5. Your Contact address:

6. Your Professional address (if different from above):

7. Your Area of specialization:

8. Would you like to review papers in events organized by VSI? :

9. How many papers are you willing to review? :

10. Your Brief bio-data: Attach separately

11. How can you contribute to the activities of VSI? :

12. What Activities would you like VSI to organize? :

13. Details of Payment:

Cash:	
DD no:	
Dated:	
Drawn on Bank:	
Amount:	

I agree to be a member of the VLSI Society of India and have read and understood the charter of the society. I will actively contribute towards the objectives of the society.

Place and Date: **Member Signature**

Category	**Membership Rates:**	
	Yearly	**5-yearly**
Student Member:	Rs. 500/=	N/A
Non-student member:	Rs. 1,000/=	Rs 4,500/-
Corporate member:	Rs. 10,000/=	Rs 45,000/-

Mail the form along with the DD to:
Mr. Gopal Naidu, Treasurer VLSI Society of India
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park, Adjacent to LRDE, C.V.Raman Nagar Post, Bangalore: 560 093
PH: 2509 9363, FAX: 91-80-2504 8213

The DD to be made out to: "VLSI Society of India" and payable at Bangalore.

- Please also enter the details in the online membership form http://vlsi-india.org/vsi/activities/reg.shtml to update records.
- Processing the card subject to the DD receipt. Please allow two weeks.
- The photograph is for official records only and will not be imaged onto the membership card.
- Students to attach college credentials.
- Inscribe **"Towards VSI Membership - New/ Renewal"** at the rear side of DD. Students to attach college credentials.
- The same form to be used for a new membership or Renewal. In the event of change of address, please update online.
- Please do not send scanned images of DD or the Form. Processing the card subject to the DD receipt. Allow two weeks.
- Become a VDAT Yahoogroup member to receive updates on all announcements. Details on http://vlsi-india.org/docs/mailgroup.shtml